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Axiomatic Design of a Chemical Mechanical Polishing (CMP) Wafer Carrier with Zoned Pressure Control

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ABSTRACT

Axiomatic Design was used to develop a complete platform for chemical mechanical polishing (CMP) of silicon wafers. A functional requirement of the machine emerging from the axiomatic design process is the control of the wafer-scale polishing uniformity. Mechanisms to maintain control of the uniformity were designed, and integrated into a wafer carrier, which holds the wafer during polishing and applies normal pressure to the polishing interface. The wafer carrier is capable of controlling the pressure in four annular zones on a 200 mm wafer, as well as the pressure of the surrounding retaining ring. Initial testing of the wafer carrier indicates a successful design, offering removal non-uniformity of 1.7% after polishing 5,700 Å of SiO_2 from the surface of a silicon wafer.

Keywords: Axiomatic, design, chemical mechanical polishing (CMP)

INTRODUCTION

The work presented in this paper was part of a research project at MIT to explore chemical mechanical polishing (CMP), then develop advanced processing methods and equipment. A custom designed polishing test-bed helped develop an understanding of the challenges in polishing thin discs as well as the influences of machine design parameters on the polishing process before the final hardware was designed and fabricated. A CAD model of the final machine is shown in Figure 1.

A set of process requirements is developed, and applied to the design or the machine. Axiomatic design, a structured design methodology, allows top-level requirements to be decomposed and satisfied until it is possible to fabricate hardware for the design. Also, the various design elements were correctly sequenced, insuring proper function of the completed design. One of the benefits of axiomatic design is the documented design process, allowing the impact of future design changes to be predicted before implementation

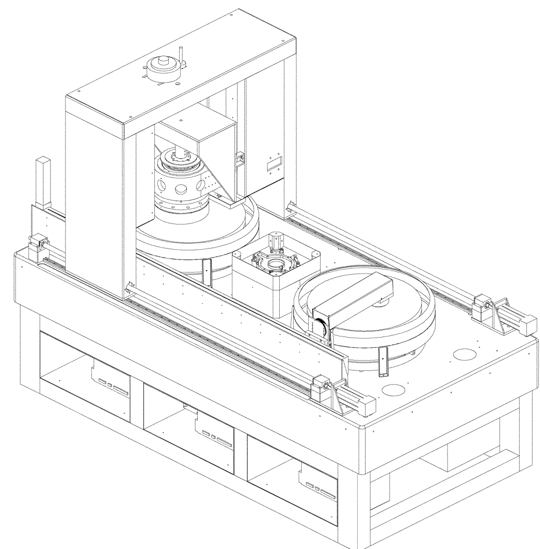

Figure 1: The MIT CMP α-machine

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Axiomatic Design

The axiomatic design process is centered on the satisfaction of functional requirements (FRs). FRs are defined as the minimum set of independent requirements that completely characterize the functional needs in the functional domain. The goal of the design is to satisfy the FRs, and this is done by creating a system that uses design parameters (DPs) to affect the behavior such that the FRs are satisfied [1].

Given a set of FRs, the designer conceives of a physical embodiment containing a DP that may be adjusted to satisfy the FR. When embodiments and DPs are selected for the design, they are chosen according to the two design axioms:

The Independence Axiom – Maintain the independence of the functional requirements.

The Information Axiom – Minimize the information content of the design.

The design matrix relates the FR vector to the DP vector. It is used to note the effects of DPs on FRs. An example design matrix is contained in the following design equation:

$$\begin{Bmatrix} FR\,1 \\ FR\,2 \end{Bmatrix} = \begin{bmatrix} A_{11} & 0 \\ A_{21} & A_{22} \end{bmatrix} \begin{Bmatrix} DP\,1 \\ DP\,2 \end{Bmatrix} \qquad (1)$$

where A_{11} denotes the effect of DP1 on FR1, A_{21} denotes the effect of DP1 on FR2, etc. When the design equations represent conceptual levels of the design, it is common for the elements of the matrix, A_{ij} to be represented with an 'X' if there is an effect, and an 'O' if there is no effect. To satisfy the Independence Axiom, the design matrix must be either diagonal or triangular. The triangular matrix in Equation 1 represents a decoupled design. For correct implementation of such a design, it is necessary to set the value of DP1 before setting the value of DP2. If the matrix in Equation 1 were diagonal, the design would be uncoupled, and the DPs may be set in any order.

Axiomatic design begins with the most general requirements of the system, and decomposes these into sub-requirements. The goal of decomposing an FR/DP pair is to develop a combination of elements that, used together, result in the parent. As the system is decomposed, it is necessary to specify a set of FRs, move to the physical domain by conceiving of a design solution, and then proceed back to the functional domain to add a level of detail. This process of moving from the functional to physical domains, and progressing from a general to a detailed description is called zigzagging.

The hierarchical collection of FRs and DPs generated during the zigzagging process is termed the system architecture. Zigzagging is repeated until it is possible to construct the system from the information contained in the system architecture.

As most DPs are invariably associated with random variations, the complexity of a decoupled system increases with the number of layers of decomposition, since the allowable variations of DPs decreases.

CMP

The CMP process is used by the semiconductor manufacturing industry as a method of smoothing topology and reducing material thickness on the surface of a wafer [2]. The CMP process widely employed uses abrasive particles mixed with a liquid to make polishing slurry, and a porous polishing pad to move the abrasive across the wafer surface. Material is removed from the wafer surface, and the process stopped when sufficient planarity has been achieved or when sufficient material has been removed. Because the entire wafer is polished at once, the wafer-scale uniformity of removal is a significant factor in evaluating the a CMP process. Also, the trend of the semiconductor industry towards larger wafers places a growing emphasis on uniformity of processing, as the potential for loss increases.

The CMP process is used in inter-level dielectric (ILD) planarization, shallow trench isolation (STI), and metal damascene. This research has been focused on one of the primary applications: copper damascene [3]. The requirements for polishing copper in a damascene process are different than those for polishing oxide during ILD planarization.

If one area of the wafer is under-polished, the metal lines will be shorted, resulting in a faulty circuit. As the wafer is polished to insure that there are no under-polished areas, there may be regions of the wafer that polish more quickly and progress past the optimal stopping point, resulting in copper loss at the device level. The performance of a CMP process at the wafer level is quantified by the Within-Wafer-Non-Uniformity (WIWNU). WIWNU is usually expressed as the standard deviation of either removed or remaining thickness divided by the mean value of the measurement. Current process requirements call for less than 5% WIWNU.

WIWNU is the primary factor that may be influenced by machine design. Because the current process uses two- or three-body abrasion, it is an averaging process that tends to smooth over the entire surface. Therefore, there is no mechanism for affecting the process within the area of a single die, let alone within each of the dies individually.

Many attempts have been made to characterize removal of material with the CMP process. Initial models used the Preston Equation [4]:

$$MRR = k_p P V \qquad (2)$$

where MRR is the material removal rate, k_p is the Preston constant, P is the local pressure, and V is the relative velocity between abrasive and pad. The Preston constant is a function of many things, including the interface conditions, slurry distribution, chemistry, etc.

Zhao and Shi have performed analysis and experimentation that shows the Preston equation is not an accurate representation of the CMP process, but rather the removal rate should include a nonlinear relationship with pressure, and that polishing does not take place below a certain threshold pressure [5, 6]. The relationship is expressed as:

$$MRR=K(V)(P^{2/3}-P_{th}^{2/3}) \qquad (3)$$

where K is a constant which depends on velocity, V, and P_{th} is now the threshold pressure. Other people have developed their own relationships for the removal rate, generally finding various dependence on pressure and velocity [7].

No matter what the exact relationship between the removal rate and process parameters, it is clear that the two primary factors to influence the removal of material from the wafer are the velocity and

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pressure. Due to the relative difficulty associated with varying the velocity across the wafer surface, the primary approach to removal control is by controlling the pressure at the polishing interface.

Pre-polished waters may not be flat and may not be of uniform thickness, and there may be misalignment between the wafer and pad axes due to machine misalignment or polishing loads. The ability of CMP equipment to tolerate such disturbances is a benefit. Increasing compliance of the wafer backing film and the pad contribute to improved uniformity, but a more compliant polishing pad results in inferior die-scale planarity. Therefore, a stiff polishing pad is often stacked on a compliant layer, forming the stacked pad used by the majority of CMP applications today. Although these advances in consumable design have allowed the user a greater range of operation conditions, the design of the polishing tool has a large impact on the pressure distribution at the polishing interface.

Existing Technology

The number of CMP systems on the market have progressed through several generations of design. This has allowed the equipment manufacturers to address deficiencies of early machines as well as the evolving demands of the industry.

CMP tools have continually improved the methods used to apply pressure, mostly through a process of trial and error. Early tools used a rigid metal plate to load the wafer against the pad. A soft backing film covering the plate provided compliance to improve wafer scale uniformity. A gimbal, or two degree-of-freedom joint, is used to accommodate misalignment of the wafer and pad. Frictional loads of polishing create a lateral force on the wafer at the pad interface. If the wafer's gimbal point is above the interface, the force will create a moment, causing the wafer to “nose dive” into the pad.

Other means of providing the compliance of a gimbal joint allow the rotation point near or at the polishing interface. One such method uses a hemispherical surface to define the bearing point. The surface is convex from the wafer carrier such that the center of rotation lies on the polishing interface. Designs of this type have been shown in the intellectual property of Applied Materials, OnTrack, and Obsidian [8,9,10].

The reason for frictional forces affecting the wafer's pressure distribution is the coupling from the method to support frictional forces to the function of applying pressure to the wafer. By decoupling the two functions, the effects may be minimized.

Although improvements in wafer carrier gimbal design may isolate the applied pressure from frictional loads, variation in pressure may be caused by wafer thickness variation. To insure even applied pressure on the back of the wafer, several techniques have been employed. One method is the formation of a pocket of water behind the wafer and carrier film, to equalize pressure behind the wafer [11]. This approach evolved into two classes of design: direct fluid pressure and fluid pressure through a membrane.

Direct fluid pressure involves creating a seal around the periphery of the water backside, and supplying the resulting cavity with pressurized fluid. This approach offers what may be the ultimate in backside pressure uniformity, but must transfer torque to the wafer through the seal. Therefore, there must be more pressure on the seal area than the rest of the wafer, introducing a source of non-uniformity and performance uncertainty. Direct fluid pressure approaches have been demonstrated by CMP users, but have not been adopted by tool manufacturers [12,13].

Fluid pressure applied through a membrane separates the wafer from a fluid reservoir. The fluid provides the pressure for polishing, while the membrane surface transmits the necessary torque to the wafer. Because the membrane is highly compliant, the pressure distribution seen on the wafer backside closely follows the uniform pressure in the cavity.

The membrane-style approach has been demonstrated in intellectual property documents from tool manufacturers [14,15]. One of the limitations is performance at the wafer edges. The edges of the membrane are coupled to the housing of the wafer carrier, limiting the compliance. It is possible to isolate the membrane from the carrier housing by providing a second pressure source to load the membrane. In effect, the secondary pressure controls the membrane “bias”, or the ratio of sidewall loading to central region loading.

Applied Materials have demonstrated in intellectual property designs of the variable bias type of membrane [16,17]. One significant advantage of this approach is the ability to control the wafer-level uniformity. The bias type membrane design is capable of adjusting the relative polish rate of the outer periphery and central area of the wafer, and as such offers the user an extended level of control over polishing. Although the bias type membrane design does offer some control of uniformity, its single bias pressure allows only rough adjustment of the radial pressure profile. There are a number of designs that attempt to offer increased spatial resolution when controlling the pressure profile. Both Applied Materials and an independent inventor have protection for concepts that provide a number of pressures [18,19]. The MIT α-machine wafer carrier was designed before the patents for such designs were issued, and while it is similar, there are advantages to the MIT design. Intellectual property protection has been filed.

THE MIT α-MACHINE WAFER CARRIER DESIGN

The MIT α-machine was designed as a complete system, and includes many elements in order to satisfy its top functional requirements. As the requirements for the CMP system were decomposed, the leaf level DPs were integrated into hardware. Two main branches of the decomposition contain elements that became part of the wafer carrier – the machine element that holds the wafer during polishing. It contains most of the design parameters for the wafer retention system, DP 1.1.1.3, and interface pressure, DP 1.1.1.5, as well as those for the uniformity control mechanisms, DP 3.2.1. Following is the decomposition of these levels, with explanation of what the design parameters are and how they interact with the functional requirements.

FR/DP1.1.1.3: Maintain wafer position - Wafer retention system

To hold the wafer during polishing, it is necessary to prevent undesired translation and rotation. These are the two requirements addressed in the decomposition of FR/DP 1.1.1.3, shown below in Table 1. The rotation of the wafer relative to the carrier is the only influence the wafer carrier may have on the velocity of the wafer relative to the pad. A schematic of the decomposition is shown in Figure 2, and the associated design equation is shown in Equation 4.

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Table 1: FR/DP 1.1.1.3 decomposition

Element #	Functional Requirements (FRs)	Design Parameters (DPs)
1.1.1.3.1	Prevent wafer translation	Wafer locating system
1.1.1.3.2	Prevent wafer rotation relative to carrier	Wafer carrier surface

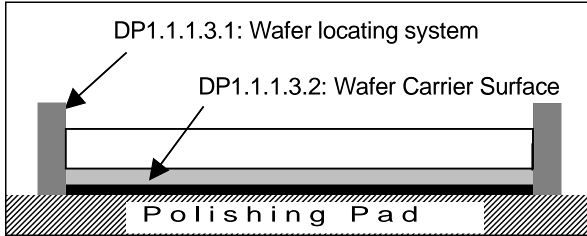

Figure 2: FR/DP 1.1.1.3 decomposition schematic

$$\begin{Bmatrix} FR1.1.1.3.1 \\ FR1.1.1.3.2 \end{Bmatrix} = \begin{bmatrix} X & O \\ O & X \end{bmatrix} \begin{Bmatrix} DP1.1.1.3.1 \\ DP1.1.1.3.2 \end{Bmatrix} \quad (4)$$

DP 1.1.1.3.1 The wafer locating system is a means for surrounding the wafer and trapping it between the polishing pad and the wafer carrier, so that polishing pressure may be applied. This FR/DP pair must be further decomposed to realize it as a physical system.

DP 1.1.1.3.2 The surface of the wafer carrier that contacts the wafer is designed to provide a high friction with the wafer back surface. This friction will prevent the wafer rotation. Commercially available CMP systems use compliant pads, called backing films, as the surface that contacts the wafer. If it is necessary to modify the surface of the wafer carrier for this design, it is possible to use such a film. This may not be necessary if it is possible to provide sufficient friction with the native surface of the carrier.

FR/DP 1.1.1.3.1: Prevent wafer translation - Wafer locating system

The wafer locating system is decomposed as shown in Table 2. The associated design equation is Equation 5, and a description of the DPs follows, along with their interactions with the FRs.

Table 2: FR/DP 1.1.1.3.1 decomposition

Element #	Functional Requirements (FRs)	Design Parameters (DPs)
1.1.1.3.1.1	Provide barrier	Ring ID – compliant
1.1.1.3.1.2	Support friction loads	Retaining ring support thickness
1.1.1.3.1.3	Maintain barrier contact with pad	Minimum ring contact pressure

$$\begin{Bmatrix} FR1.1.1.3.1.1 \\ FR1.1.1.3.1.2 \\ FR1.1.1.3.1.3 \end{Bmatrix} = \begin{bmatrix} X & O & O \\ O & X & O \\ O & X & X \end{bmatrix} \begin{Bmatrix} DP1.1.1.3.1.1 \\ DP1.1.1.3.1.2 \\ DP1.1.1.3.1.3 \end{Bmatrix} \quad (5)$$

DP 1.1.1.3.1.1: The ring ID is the inner surface of the retaining ring, which contacts the edge of the wafer. It is this surface which provides the support to prevent wafer translation. By controlling the compliance of the inner surface, it is possible to provide a barrier that will not damage the wafer. Here the choice is a material selection issue. The material must be compatible with the chemical and mechanical environment that will be present. Use of a very soft material will result in excessive wear of the retaining ring and therefore frequent maintenance requirements.

DP 1.1.1.3.1.2: The retaining ring support thickness is a mechanical parameter to control the structural strength of the assembly used to support the retaining ring. The ring support thickness affects FR 1.1.1.3.1.3 because the influence of external disturbances on the retaining ring may influence its ability to maintain contact with the pad. An easily deflected ring will require a higher minimum pressure to avoid breaking contact with the pad under disturbance.

DP 1.1.1.3.1.3: The minimum contact pressure is the interface conditions around the bottom surface of the ring. To maintain contact with the pad, the contact pressure must be maintained above a certain value. This value is determined experimentally, as the theoretical minimum is zero, such that physical proximity is maintained. DP 1.1.1.3.1.3 is a threshold variable, and is satisfied by a range of values. The actual contact pressure of the retaining ring will be set by the requirements for edge effect control, to pre-compress the polishing pad, as shown later in FR/DP 3.2.1.1.

FR/DP1.1.1.5: Apply normal pressure - Interface pressure

Pressure is one of the key variables to influence the removal of material from the wafer surface, and is primarily influenced by the design of the wafer carrier. By using a flexible membrane to form a closed bladder, pneumatic pressure within the bladder guarantees uniform pressure is applied to the wafer, as described in Existing Technology above. The decomposition of FR/DP 1.1.1.5 is shown in Table 3. The associated design equation is shown in Equation 6, and a schematic of the DPs is shown in Figure 3. Following is a description of each of the DPs, and their relationships with other FRs, explaining the off-diagonal elements in the design matrix.

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Table 3: FR/DP 1.1.1.5 decomposition

Element #	Functional Requirements (FRs)	Design Parameters (DPs)
1.1.1.5.1	Provide pressure	Nominal compartment pressure
1.1.1.5.2	Create local pressure variation	Pad surface modulus; $E_{PAD\text{-}TOP}$
1.1.1.5.3	Accommodate wafer form variation	Stack stiffness; $(Eh^4)_{mem} + (E_{bulk}/h)_{PAD}$
1.1.1.5.4	Transmit pressure to interface	Membrane area
1.1.1.5.5	Accommodate machine misalignment	Isolation bellows stiffness
1.1.1.5.6	Support normal loads	Normal load support chain

$$\begin{Bmatrix} FR\,1.1.1.5.1 \\ FR\,1.1.1.5.2 \\ FR\,1.1.1.5.3 \\ FR\,1.1.1.5.4 \\ FR\,1.1.1.5.5 \\ FR\,1.1.1.5.6 \end{Bmatrix} = \begin{bmatrix} X & O & O & O & O & O \\ O & X & O & O & O & O \\ O & X & X & O & O & O \\ O & O & O & X & O & O \\ O & O & X & O & X & O \\ O & O & O & X & O & X \end{bmatrix} \begin{Bmatrix} DP\,1.1.1.5.1 \\ DP\,1.1.1.5.2 \\ DP\,1.1.1.5.3 \\ DP\,1.1.1.5.4 \\ DP\,1.1.1.5.5 \\ DP\,1.1.1.5.6 \end{Bmatrix} \quad (6)$$

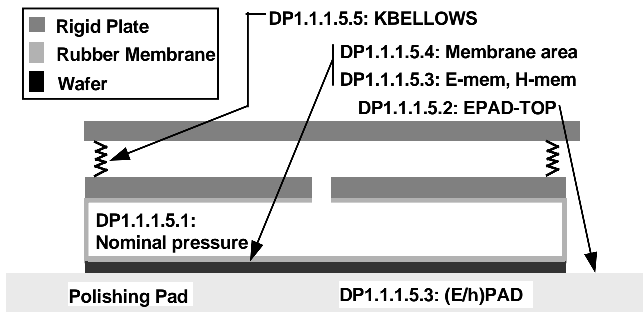

Figure 3: FR/DP 1.1.1.5 decomposition schematic

DP 1.1.1.5.1: Compartment pressure is the pressurized gas supplied to the bladder compartment. This pressure is controlled with a E/P (voltage to pressure) valve, using a control loop within the valve. Since the pressure is supplied to a closed cavity, there will be a uniform pressure within the cavity, ensuring the ability to provide a known pressure to the back of the wafer. Earlier designs for CMP systems used mechanical force to apply pressure to the wafer, and relied on compliant pads to create a uniform pressure distribution. Such methods are sensitive to the manufacturing tolerances of the pads as well as incoming wafer variation. With the extremely flexible membrane used in this design, uniform pressure is easily obtained.

DP 1.1.1.5.2: The pad surface modulus is what creates preferential removal of the high features compared to the low features – the process of planarization. At the length scale of the features being polished (less than one micron), macroscopic features of the pad have little effect. The pad appears to be a semi-infinite, elastic solid that supports rigid particles. The pad surface modulus affects FR 1.1.1.5.3 because a higher modulus will, to some extent, reduce the ability of the system to tolerate wafer form variation.

DP 1.1.1.5.3: $(E/h)_{PAD}$ is the stiffness of the pad in the vertical direction. The membrane modulus, E_{mem}, combined with the membrane thickness, h_{mem}, describes the bending stiffness of the planar membrane. The total stack stiffness of the pad and membrane controls how the pressure will respond to wafer form variation. A low stiffness will accommodate a large wafer form variation without creating large pressure variation. Due to the high compliance of the membrane used to apply pressure to the wafer, the primary concern here is from the pad side of the wafer. Generally, the pad thickness may be used to control the stack stiffness in a way that will not influence polishing at a local level. Most pads used in commercial processes use a multi-layer stack, so that the surface presented to the wafer is of the desired modulus to satisfy DP 1.1.1.5.2, and then an additional lower layer may be used to reduce the overall stack stiffness to a value suitable for robustness to incoming wafer variation. The stiffness affects FR 1.1.1.5.5 because low stiffness reduces requirements for misalignment, as low pad stiffness creates less pressure variation due to misalignment.

DP 1.1.1.5.4 - Membrane area is the overall area of the membrane; It should match the wafer area. Membrane area affects FR 1.1.1.5.6 because a change in area will change the applied loads that the system must support. The area does not change during operation of the machine, so creates no problem.

DP 1.1.1.5.5 - The isolation bellows stiffness is the tip-tilt stiffness of the bellow used to decouple the wafer carrier membrane from the rest of the wafer carrier. Thus, any misalignment in the wafer carrier itself will not translate into a pressure variation on the wafer surface. This decoupling bellows has the benefit of isolating the normal loads on the wafer, i.e. the polishing pressure, from frictional loads that are supported by the wafer carrier. This is a major advantage over some earlier CMP systems, in which a strong coupling exists.

DP 1.1.1.5.6 - The load support chain is the series of machine elements that allows a load to be present at the wafer-pad interface without undue deflection. These are primarily load ratings of the various hardware components used in the mechanical system, and have little influence on the wafer carrier itself.

With the collection of FRs and DPs shown in Table 3 along with the rest of the necessary elements, the design satisfies the minimum requirements to polish wafers. It can supply pressure to the wafer, and does so in a manner that is tolerant of input variation. This type of design was reached in most commercial CMP equipment by the second or third generation. The desire in this project was to extend the capabilities of the machine past the current state-of-the-art. To realize these goals, a top level FR was created to maximize the output of the machine. As a sub requirement of the output, it was necessary to maximize the yield of the machine when polishing a single wafer. To maximize yield, a sub-FR is to minimize the amount of overpolishing when processing wafers. The decomposition and realization of this FR follows.

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FR/DP 3.2.1: Minimize overpolish percentage - Uniformity control mechanisms

To minimize the overpolishing of wafers, the only option is to improve uniformity. This decision is made with the assumption that the optimal endpoint is correctly used, meaning that some areas on the wafer are correctly polished, and some are overpolished. The decomposition of FR/DP 3.2.1 is shown in Table 4, along with the associated design matrix in Equation 7, and a schematic of the elements in Figure 4. Following is a description of the DPs and their relationships to the FRs, explaining the elements in Equation 7.

Table 4: FR/DP 3.2.1.1 decomposition

Element #	Functional Requirements (FRs)	Design Parameters (DPs)
3.2.1.1	Control edge effects	Retaining ring pressure
3.2.1.2	Control polish rate as a function of radius	Radial pressure distribution

$$\begin{Bmatrix} FR\ 3.2.1.1 \\ FR\ 3.2.1.2 \end{Bmatrix} = \begin{bmatrix} X & O \\ X & X \end{bmatrix} \begin{Bmatrix} DP\ 3.2.1.1 \\ DP\ 3.2.1.2 \end{Bmatrix} \quad (7)$$

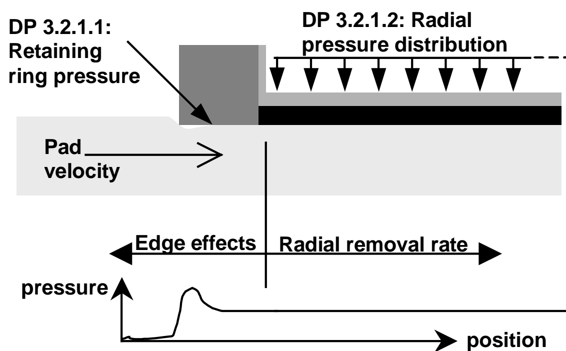

Figure 4: FR/DP 3.2.1 decomposition schematic

DP 3.2.1.1: The retaining ring is an element of the machine which originally satisfies the functional requirement to maintain the wafer position during polishing (FR 1.1.1.3.1). When the DP for uniformity control mechanisms (DP 3.2.1) is introduced, the existing hardware element of the retaining ring is used to control the edge effects, by controlling the normal pressure against the polishing pad. As long as it remains above the minimum pressure (DP 1.1.3.1.3), this pressure has no effect on the ability of the retaining ring to maintain the wafer position during polishing, so functional independence is maintained. By making the retaining ring pressure approximately equal to the pressure at the polishing interface, the edge effects which would have occurred near the wafer are pushed out onto the retaining ring, a non-critical surface. The retaining ring pressure affects FR 3.2.1.2 because if it is too low or too high, the edge effects influence the wafer, and may be partially compensated by a mechanism to vary the removal rate in the radial direction. Since it is not possible to control the pressure under the retaining ring with the existing hardware, it is necessary to further decompose FR/DP 3.2.1.1.

DP 3.2.1.2: The radial pressure distribution directly affects the removal rate on the wafer. Since the wafer is rotating during polishing, the removal tends to be axisymmetric, and control is only needed in the radial direction. As shown in Equations 2 and 3, pressure and velocity are the primary influences on the removal rate. Due to the polishing kinematics, the only effect of changing velocity is to increase the removal rate at the edge of the wafer relative to the center, with a linear transition between the two regions. Therefore, pressure is the parameter selected to control the removal rate. The means of controlling the pressure distribution as a function of wafer radius will be decomposed further in a following section.

FR/DP 3.2.1.1: Control edge effects - Retaining ring pressure

The pressure under the retaining ring is controlled by connecting the retaining ring to the machine spindle through a flexure. By monitoring the strain in the flexure during polishing, and adjusting the vertical position of the spindle, the force on the retaining ring may be controlled. Alternatives to the flexure element might be an externally pressurized radial fluid bearing. While this system would satisfy the functional requirements, it involves significantly more complexity than the flexure design. The flexure was chosen for its lack of moving parts and ease of fabrication. The decomposition of FR/DP 5.2.1.1 is show below, in Table 5, along with the associated design matrix in Equation 8 and a schematic of the system in Figure 5. Following is a description of the individual DPs, and the interactions they have with the FRs.

Table 5: FR/DP 3.2.1.1 decomposition

Element #	Functional Requirements (FRs)	Design Parameters (DPs)
3.2.1.1.1	Accommodate head-pad misalignment	Retaining ring flexure O.D.
3.2.1.1.2	Measure force from flexure	Retaining ring flexure strain
3.2.1.1.3	Control force from flexure	Z-Axis position during polish

$$\begin{Bmatrix} FR\ 3.2.1.1.1 \\ FR\ 3.2.1.1.2 \\ FR\ 3.2.1.1.3 \end{Bmatrix} = \begin{bmatrix} X & O & O \\ X & X & X \\ O & X & X \end{bmatrix} \begin{Bmatrix} DP\ 3.2.1.1.1 \\ DP\ 3.2.1.1.2 \\ DP\ 3.2.1.1.3 \end{Bmatrix} \quad (8)$$

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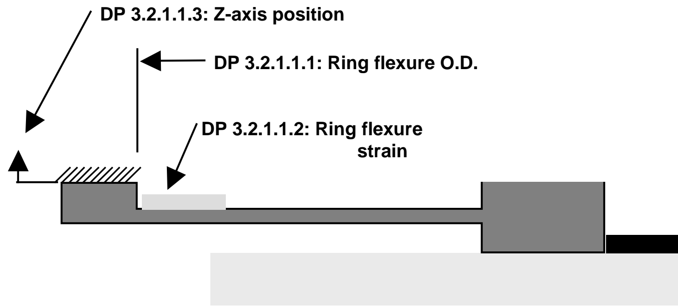

Figure 5: FR/DP 3.2.1.1 decomposition schematic

DP 3.2.1.1.1: The retaining ring flexure O.D. is the outer diameter of the annular flexure. The inner diameter is constrained to fit the retaining ring, which surrounds the wafer. By controlling the O.D. of the flexure, sufficient tip-tilt compliance can be incorporated to tolerate some misalignment. Since the ring flexure is part of a precision machine, even one degree of misalignment would be a large amount, so the requirement is relatively easy to satisfy. In the MIT α-machine, the O.D. is 11.150", and the I.D. is 10.1". Flexure thickness is 0.025". The flexure O.D. influences FR 3.2.1.1.2 because the O.D. changes the relationship between force and strain, and therefore must be designed before the appropriate range of strain is known.

DP 3.2.1.1.2: The retaining ring flexure strain is measured using a strain gage applied to the upper surface of the flexure, on the outer perimeter. The gage is temperature compensated for the material it is mounted on to minimize thermal drift, and calibrated before polishing is started, as the ring contacts the pad. The flexure strain affects FR 3.2.1.1.3 because a change in the strain necessitates a change in the control effort.

DP 3.2.1.1.3: The Z-axis position during polish directly controls the separation of the spindle from the pad, and therefore is used to maintain the desired force on the ring flexure. The Z-axis position influences FR 3.2.1.1.2 because when the spindle height changes, the strain is a measure of the change. During polishing, the machine software measures the value for strain and adjusts the Z-axis position to compensate for error from the desired value. This forms a servo feedback system, and thus, the apparent coupling in the design is managed.

FR/DP 3.2.1.2: Control radial polish rate - Radial pressure distribution

The other uniformity control mechanism in the decomposition of FR/DP 3.2.1 is the radial pressure distribution. The method to satisfy this FR must be compatible with the system to control the interface pressure (FR/DP 1.1.1.5). The pressure distribution is controlled by dividing the membrane used in the FR/DP 1.1.1.5 decomposition into annular zones, and then controlling the pressure in each of the zones. The flexible membrane that applies pressure is compatible with such an approach allowing integration of the hardware elements. The decomposition of requirements is shown in Table 6. In order to vary the pressure as a function of radius, it is necessary to somehow create compartments behind the membrane that pushes on the wafer – this is FR 3.2.1.2.1. Here is where design alternatives emerge with significant differences. One possibility that was considered is shown in Figure 6. The membrane has been divided into closed compartments separated by walls made of the same elastomer as the membrane. While this is a good starting place, it has significant problems. At each dividing wall, there is a large discontinuity of the pressure applied to the membrane, which will result in difficulty when trying to control the pressure transition between segments (FR 3.2.1.2.4).

Rather than the solid dividing walls shown in Figure 6, the final design for the MIT α-machine uses walls with a hollow cross section. This gives the walls a much higher compliance, and allows them to contain an internal pressure. The internal pressure of the dividing walls insures a smooth transition from one segment to the next. By introducing vents that connect the dividing wall with each adjacent segment, the pressure in the dividing wall is automatically maintained at an average of the bordering segments. A schematic of the final design is shown in Figure 7. The decomposition of the radial pressure distribution is shown in Table 6, with the associated design matrix in Equation 9 and a schematic of the elements in Figure 7. Following is a description of the DPs, and their interaction with the FRs.

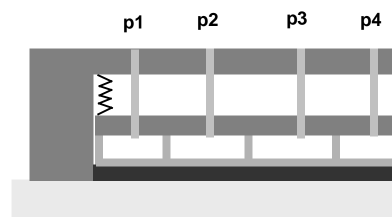

Figure 6: One alternative for FR/DP 3.2.1.2

Table 6: FR/DP 3.2.1.2 decomposition

Element #	Functional Requirements (FRs)	Design Parameters (DPs)
3.2.1.2.1	Divide wafer area into segments	Membrane compartment areas
3.2.1.2.2	Control applied pressure profile	Compartment pressure distribution
3.2.1.2.3	Smooth applied pressure profile	Membrane thickness; h-mem
3.2.1.2.4	Control transition between segments	Compartment divider vent length & I.D.

$$\begin{Bmatrix} FR\,3.2.1.2.1 \\ FR\,3.2.1.2.2 \\ FR3.2.1.2.3 \\ FR\,3.2.1.2.4 \end{Bmatrix} = \begin{bmatrix} X & O & O & O \\ X & X & O & O \\ O & O & X & O \\ O & X & X & X \end{bmatrix} \begin{Bmatrix} DP\,3.2.1.2.1 \\ DP\,3.2.1.2.2 \\ DP\,3.2.1.2.3 \\ DP\,3.2.1.2.4 \end{Bmatrix} \quad (9)$$

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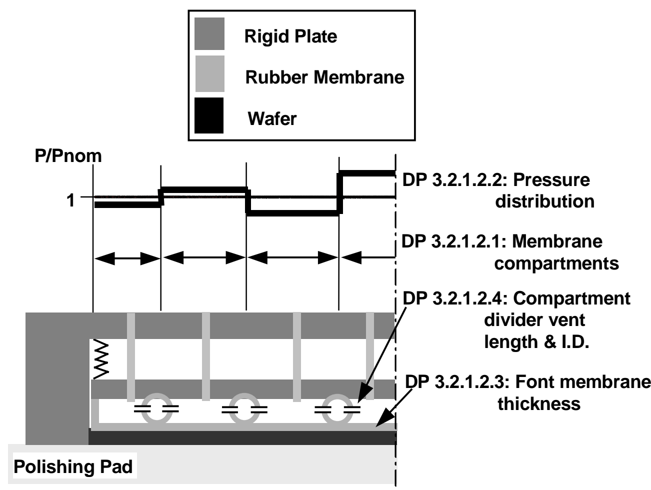

Figure 7: FR/DP 3.2.1.2 decomposition schematic

DP 3.2.1.2.1: The membrane compartment areas are a means for applying a pattern of displacement in concentric rings to the wafer front surface. With this displacement, the wafer front side will see a variation in normal pressure due to the compression of the polishing pad. The compartments divide the total wafer area into independently controllable regions. Because the variation in removal rate tends to show the highest spatial variability near the edge of the wafer, the outermost compartment has a smaller radial dimension than the others. The membrane compartments affect FR 3.2.1.2.2 because the way the total area is divided into segments defines how the profile is controlled.

DP 3.2.1.2.2: The compartment pressure distribution is the pressure supplied to a particular membrane compartment to load the respective area of the wafer. Each individual compartment pressure is defined as a ratio to the nominal pressure (DP 1.1.1.5.1). The pressure distribution affects FR 3.2.1.2.4 because the difference between adjacent compartments determines how much of a transition there is to smooth out, although certain assumptions may be made to complete the design of the wafer carrier.

DP 3.2.1.2.3: The front membrane thickness may be used to smooth the pressure distribution as it is transmitted to the wafer back surface. The front membrane thickness is coupled to the following FRs: 3.2.1.2.4: The membrane thickness will smooth out the discontinuities of pressure at the dividing walls, and so make the system more tolerant to such discontinuities. The maximum allowed variation across a transition from one compartment to the next is therefore influenced by the membrane thickness.

DP 3.2.1.2.4: The compartment divider vent length & I.D. are the characteristics that define flow through the vents into each compartment divider. The divider is formed of a tubular cross section, and therefore may contain a pressure that is an average of the adjacent compartment. The tubular cross section gives the divider a high compliance, so the pressure within it dominates the pressure applied to the wafer backside.

Detailed design

The wafer carrier elements identified in the system architecture were integrated into hardware elements. The result is shown below in Figure 7, a CAD drawing of the assembled system.

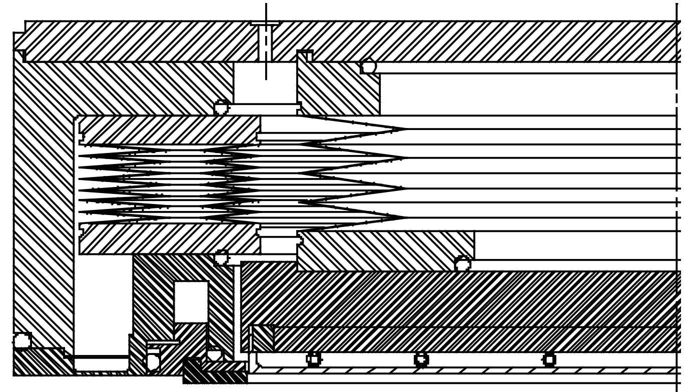

Figure 8: CAD drawing of the wafer carrier showing the integration of leaf level DPs.

TESTING & EVALUATION

The MIT α-machine wafer carrier was evaluated by polishing SiO_2 blanket wafers with industry standard process conditions. The wafers are 200 mm silicon wafers with 1 μm of CVD TEOS oxide. Polishing was done using a Rodel IC-1400 K-groove pad and Rodel Klebosol® 1501-50 slurry. Wafers were polished for two minutes at 160 ft/min (0.8 m/sec) relative velocity and 5 psi (34.5 kPa). The pad was conditioned using a diamond abrasive between wafers. Wafers were measured using an optical interferometer to sample 49 points per wafer.

First, wafers were polished using no pressure distribution in the membrane compartments. An equal nominal pressure of 5 psi was applied to each compartment. The removal non-uniformity was 16.9%. The removal was concentrated towards the center of the wafer, as shown in Figure 9. To investigate the ability of the segmented membrane to control the removal rate, pressures in the compartments were adjusted to achieve maximum uniformity. The pressure ratios relative to the 5 psi nominal pressure were 1.0, 1.05, 1.10, and 1.25, from the center of the wafer to the edge.

With manual adjustment of the pressures in the compartments, the wafer carrier was able to achieve a removal non-uniformity of 1.7% while maintaining a removal rate of 2,850 Å/min. The resulting oxide thickness is shown in Figure 10. A more detailed map of the surface is shown in Figure 11.

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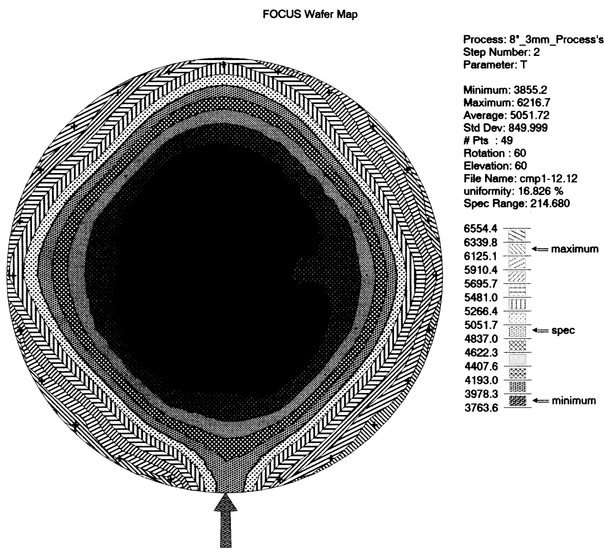

Figure 9: Plot of SiO_2 film thickness after polishing with uniform compartment pressure of 5 psi. Removal non-uniformity is 16.8%.

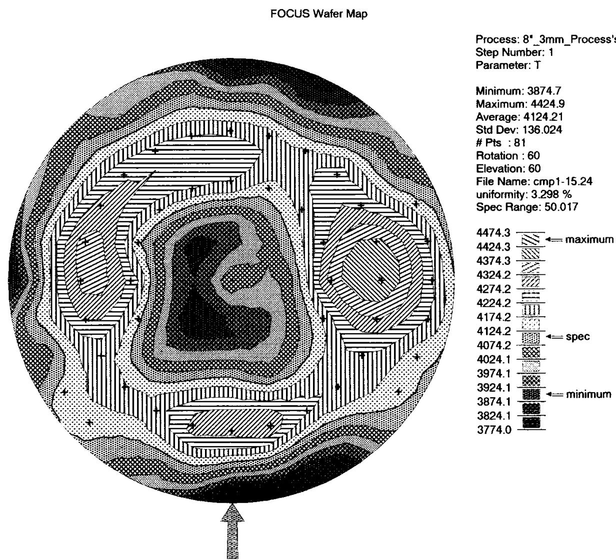

Figure 10: Plot of SiO_2 film thickness after polishing with adjusted compartment pressures.

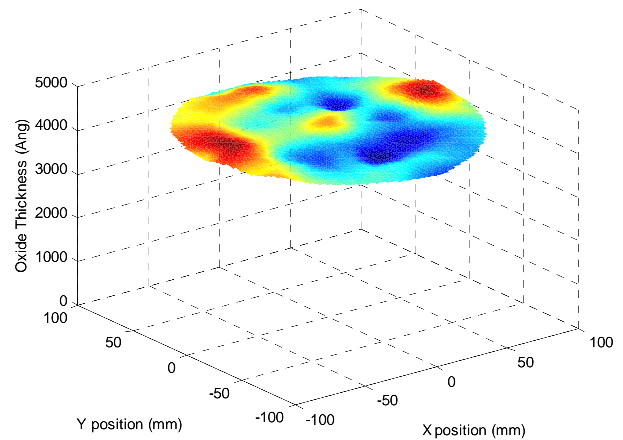

Figure 11: Plot of the remaining SiO_2 thickness after 120 sec. polish at 5 psi. Removal non-uniformity is 1.7%.

CONCLUSIONS

The design presented in this paper is a successful approach to a CMP wafer carrier. The system for controlling removal rate allowed the MIT α-machine to produce wafers with excellent non-uniformity, exceeding the demands of the industry at the time of the design. It has shown added control of the process as designed, and may be used as part of a system to satisfy the needs of the semiconductor industry.

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