Analysis of the Transistor Cascode Configuration

By J. R. James*

Fixed component neutralization as used in the production of tuned amplifiers is often difficult to achieve, due to the spread in transistor parameters. A transistor cascode amplifier does not require neutralization but has less gain than two stages in the grounded emitter configuration. This article investigates to what extent the internal feedback and gain are reduced.

(Voir page 62 pour le résumé en français: Zusammenfassung in deutscher Sprache Seite 66)

FIRST the Y parameters (see Appendix 1) of the grounded emitter amplifier will be compared with those of the cascode amplifier. The relationship between the two configurations is established using matrix algebra. Also the theoretical reduction in the gain and internal feedback of the cascode configuration is derived. Next a practical case will be considered in order to verify the theoretical relationships and finally the use of the circuit will be discussed.

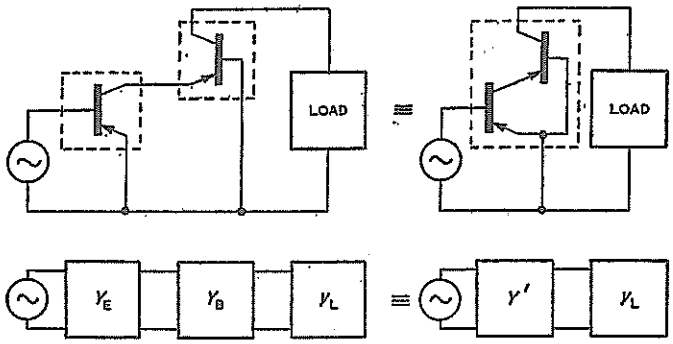

Fig. 1. The cascode configuration considered as a composite transistor

Derivation of the Y Parameters of a Cascode Amplifier from the Grounded Emitter and Grounded Base Parameters

It is assumed that the Y parameters of the transistors to be used have been measured, at the desired working point and frequency of operation, for both grounded emitter and grounded base configurations. Let them be Y_E and Y_B respectively where, in matrix form:

$$(Y_E) = \begin{vmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{vmatrix} \text{ and } (Y_B) = \begin{vmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{vmatrix}$$

Fig. 1 shows how the cascode configuration can be regarded as a grounded emitter amplifier in cascade with a grounded base amplifier. The network presentation is also shown.

As shown in Appendix 2, the A matrix of the cascode circuit can be derived from the product of the A matrices of the grounded emitter and grounded base configurations. Therefore first of all the Y matrices (Y_E) and (Y_B) must be converted into the A matrices (A_E) and (A_B). The following notation will be used:

$$(A_E) = \begin{vmatrix} A & B \\ C & D \end{vmatrix} \quad (A_B) = \begin{vmatrix} a & b \\ c & d \end{vmatrix}$$

Then, if (A') is the A matrix of the cascode amplifier:

$$(A') = (A_E)(A_B) = \begin{vmatrix} Aa+Bc & Ab+Bd \\ Ca+Dc & Cb+Dd \end{vmatrix}$$

On writing the elements of the A matrices in terms of the measured Y parameters (see Appendix 1):

$$(A') = \begin{vmatrix} \dfrac{y_{22}\{Y_{22}+y_{11}\} - y_{12}y_{21}}{Y_{21}y_{21}} & \dfrac{\{Y_{22}+y_{11}\}}{Y_{21}y_{21}} \\ \dfrac{Y_{11}y_{22}\{Y_{22}+y_{11}\} - Y_{12}Y_{21}y_{22} - Y_{11}y_{12}y_{21}}{Y_{21}y_{21}} & \dfrac{Y_{11}\{Y_{22}+y_{11}\} - Y_{12}Y_{21}}{Y_{21}y_{21}} \end{vmatrix}$$

Using once again the relationship between the A and Y matrices the Y matrix (Y') of the cascode amplifier can be formed from the elements of the A matrix (A').

$$(Y') = \begin{vmatrix} \dfrac{Y_{11}\{Y_{22}+y_{11}\} - Y_{12}Y_{21}}{\{Y_{22}+y_{11}\}} & \dfrac{-Y_{12}y_{12}}{\{Y_{22}+y_{11}\}} \\ \dfrac{-y_{21}Y_{21}}{\{Y_{22}+y_{11}\}} & \dfrac{y_{22}\{Y_{22}+y_{11}\} - y_{12}y_{21}}{\{Y_{22}+y_{11}\}} \end{vmatrix}$$

In order to simplify the expression the following approximations are used:

(1) $\{Y_{22} + y_{11}\} \simeq y_{11}$

(2) $Y_{11} \gg Y_{12}$

(3) $y_{11} \simeq -y_{21}$

It can be shown[1] using H parameters that $h_{21} = (y_{21}/y_{11}) = -\alpha$. Now the current gain α of a grounded base amplifier is almost unity. Therefore $y_{11} \simeq -y_{21}$.

(Y') is now simplified as follows:

$$(Y') = \begin{vmatrix} Y_{11} & Y_{12}(y_{12}/y_{21}) \\ Y_{21} & y_o \end{vmatrix}$$

where $y_o = y_{22} - \dfrac{y_{21}\,y_{12}}{Y_{22} + y_{11}}$

The expression for the Y matrix of the cascode amplifier will now be used to investigate stability and gain.

The Stability Factor of a Cascode Amplifier

Using the derived Y parameters for the cascode configuration, the stability factor (Appendix 3) is evaluated in terms of the load admittance. A typical cascode stage operating in a multi-stage amplifier is shown in Fig. 2. It has the following features:

(1) The load admittance Y_L is a variable in the hands of the designer. It is controlled by the inter-stage transformer ratio.

(2) Reactive components across input and output terminals are tuned out at the centre frequency f_c of the pass-band.

(3) The input is driven from a constant current source. This simulates the preceding stage which is assumed

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to be another cascode amplifier with almost zero output admittance.

Derivation of Required Transfer Functions of the Amplifier

It is now convenient to derive expressions for the internal voltage feedback ratio and the forward voltage gain of a cascode amplifier with load. The power gain is also extracted and will be used later.

The A matrix (A'') for the amplifier with load is given by:

$$(A'') = (A')(a) = \begin{vmatrix} A' & B' \\ C' & D' \end{vmatrix} \begin{vmatrix} 1 & 0 \\ Y_L & 1 \end{vmatrix} = \begin{vmatrix} A'+B'Y_L & B' \\ C'+D'Y_L & D' \end{vmatrix}$$

(A') and (a) are the A matrices of the cascode configuration and load admittance Y_L.

$$\text{Voltage gain} = V_2/V_1 = \frac{1}{\{A' + B'Y_L\}} \quad \text{Since } I_2 = 0$$

$$\text{Current gain} = \frac{Y_L}{\{C' + D'Y_L\}}$$

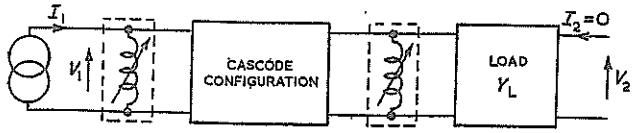

Fig. 2. The input and output circuits of a typical cascode amplifier

$$\text{Power gain} = \text{Voltage gain} \times \text{Current gain} = \frac{Y_L}{\{A'+B'Y_L\}\{C'+D'Y_L\}}$$

Using H parameters[1] it can be shown that:

$$V_1/V_2|_{I_1=0} = H_{12} = \{A'+B'Y_L\} - (B'/D')\{C'+D'Y_L\}$$

As one is driving from a constant current generator H_{12} can be taken as the fraction of voltage fed from output to input terminals.

Stability Factor S

S is now given. (Re denoting real part)

$$S = \text{Re}\left\{\frac{1}{H_{12}\{\text{voltage gain}\}}\right\} = \text{Re}\left\{\frac{D'}{D' - B'\{C'+D'Y_L\}\{A'+B'Y_L\}}\right\}$$

The A matrix (A') of the cascode configuration is now written in terms of the Y parameters derived previously.

$$(A') = \begin{vmatrix} A' & B' \\ C' & D' \end{vmatrix} = \begin{vmatrix} -(y_o/Y_{21}) & -(1/Y_{21}) \\ \dfrac{\{Y_{11}y_o - Y_{21}Y_{12}(y_{12}/y_{21})\}}{-Y_{21}} & -(Y_{11}/Y_{21}) \end{vmatrix}$$

On writing S in terms of the Y parameters and taking $y_o = 0$ and the real parts of Y_{11} and Y_L:

$$S = \text{Re}\left\{\frac{y_{21}G_{11}}{Y_{12}Y_{21}y_{12}}\right\} G_L = kG_L \qquad k = \text{Re}\left\{\frac{y_{21}G_{11}}{Y_{12}Y_{21}y_{12}}\right\}$$

The stability factor has been expressed in terms of G_L and a constant, at the frequency of resonance f_o of the input and output circuits. The amplifier will oscillate when $G_L k = 1$, the frequency of oscillation being slightly removed from f_o.

From the analysis it may be concluded, therefore, that the load conductance is determined by the stability factor desired. The derived expression for S becomes inaccurate for smaller values of G_L.

The Power Gain of the Cascode Amplifier

In order to acquire a figure of merit for the cascode configuration a comparison is made with the power gain of the grounded emitter configuration (Appendix 3).

Using the expression derived in the previous section and writing it in terms of Y parameters:

$$\text{Power gain of cascode amplifier} = \frac{|Y_{21}|^2 G_L}{\left\{G_{11}y_o - \dfrac{Y_{21}Y_{12}y_{12}}{y_{21}} + G_{11}G_L\right\}\{y_o + G_L\}}$$

$$\text{Putting } y_o = 0 \text{ and } \frac{Y_{21}Y_{12}y_{12}}{y_{21}} = 0$$

$$\text{Power gain} = \frac{|Y_{21}|^2}{G_{11}G_L} = P_o$$

The power gain P_o of a grounded emitter amplifier is:

$$P_e = \frac{|Y_{21}|^2}{4G_{11}G_{22}}$$

K is defined as follows:

$$K = 10 \log (P_o/P_e) = 10 \log 4n_1$$

where $n_1 = (G_{22}/G_L)$

When $n_1 = 1 \quad K = 6\text{dB}$

$n_1 = 2 \quad K = 9\text{dB}.$

The expression for K increases in inaccuracy as n_1 is increased.

Evaluation of a Practical Case

Using the relationships between G_L, gain and stability, an estimation of cascode stability at a given gain can be produced which will be increasingly pessimistic with increasing gain, due to the approximations made in the analysis.

For example the stability factor which allows the cascode amplifier to have 25 per cent less gain than two stages of conventional grounded emitter amplification is given by:

$$S = \text{Re}\ \{(y_{21}/y_{12}) \cdot (Y_{21}/Y_{12})\}\ 1/\{P_o\}^{3/2}$$

$$\text{Since } G_L = 4G_{22}/\{P_o\}^{\frac{1}{2}}$$

For the type SB346 at 20Mc/s, $P_o \simeq 34$

$$G_L = 0{\cdot}68\ G_{22}$$

$$S \simeq 6$$

Due to measuring errors in the Y parameters and approximations made above, the calculation of S is liable to large errors and is only quoted as approximate. A value of 6 is quite adequate for most amplifiers.

Summary of Results of the Analysis

(1) The cascode input admittance is practically equal to that of a grounded emitter amplifier.

(2) A similar result applies to Y_{21}.

(3) The output admittance is practically equal to h_{22} and for most cases can be assumed to be zero. However, as the stability factor of the amplifier is made smaller, negative conductance appears at the output terminals in shunt with h_{22} (h_{22} is the output admittance of a grounded base amplifier with the input terminal open circuited. It can be shown that $h_{22} = y_{22} - (y_{12}y_{21})/y_{11}$).

(4) The internal feedback in the cascode configuration is typically one-fiftieth of that in the unneutralized grounded emitter configuration.

(5) The cascode amplifier can only be treated as unilateral at lower gain levels. The stability factor is inversely

proportional to the gain. For a given stability factor the gain is fixed.

(6) As the stability factor is lowered, the output admittance becomes increasingly negative. A point is reached where the bandwidth is noticeably reduced. If an amplifier is designed around this operating point, the bandwidth will be very dependent on individual transistors, and also the response curves will not be additive in the normal manner.

(7) The calculation of this operating point from the analysis requires very accurate values of the Y parameters and it is believed that the experimental approach is more accurate.

Consideration of a Practical Case to Verify Analysis

Two transistors of the type SB346 were measured at $I_o = -0{\cdot}25$mA, $V_o = -3$V at a frequency of 20Mc/s. The averages of the two sets of readings are as follows with all admittances in millimhos.

	Grounded Emitter	Grounded Base	
Y_{11}	1·14 + j1·43	6·48 − j3·11	y_{11}
Y_{22}	0·32 + j0·71	0·32 + j0·71	y_{22}
$-Y_{12}$	0·08 + j0·26	0·35 + j0·71	$-y_{12}$
$-Y_{21}$	−3·42 + j5·03	6·28 − j3·14	$-y_{21}$

From the measurements the following points are apparent: :

(1) $Y_{22} = y_{22}$

(2) $-y_{12} \simeq y_{22}$

(3) $y_o = y_{22} - \dfrac{y_{21}y_{12}}{y_{11} + Y_{22}} \simeq 0$

This result is subject to accumulative measuring errors.

(4) $y_{11} \simeq -y_{21}$

(5) The maximum unilateralized matched gain in the grounded emitter configuration, based on average values is 14·3dB.

Using the measured data it was decided to test the conditions suggested in the analysis. The operating point is not optimum for the stability power gain product and thus the results are slightly pessimistic for SB346 transistors.

The optimum collector current would be about 0·5mA.

The Design of a Cascode Amplifier with $G_L = G_{22}$

Design Details

Centre frequency 20Mc/s
Bandwidth per tuned circuit 2Mc/s
Overall bandwidth (2 tuned circuits) ..... 1·3Mc/s
Transformer ratio ..... 2·4:1
Unloaded Q (Q_U) 26
Loaded Q (Q_L) 10
Added capacitance (C) 21pF
Loss per coil ..... 4·2dB

Using 26 s.w.g. enamelled wire and tunable ferrite cup cores, the primary winding was 12 turns and the secondary 5 turns.

The ferrite cup cores had considerable loss at 20Mc/s and the following comment is in order. In conventional grounded emitter amplifiers maximum gain is always achieved when the reflected load resistance is made equal to the collector output resistance, independent of any shunt coil loss resistance. Lossy coils reduce the gain and improve the stability factor.

In the following experiments the pre-determined value of resistance presented to the collector circuit is composed of both coil loss and reflected load resistance. The stability factor which is dependent on G_L is not influenced by the coil loss that only reduces the power gain of the cascode amplifier.

Results of Measurements

The amplifier was stable and easily adjusted. The bandwidth appears quite normal indicating that the negative output admittance is of a small order.

Overall bandwidth ..... 1·45Mc/s
Overall gain ..... 11·3dB
Overall gain of cascode amplifier without losses .. 19·7dB
Maximum gain of grounded emitter amplifier ....14·3dB

The difference in gain of 5·4dB is very close to the predicted value of 6dB.

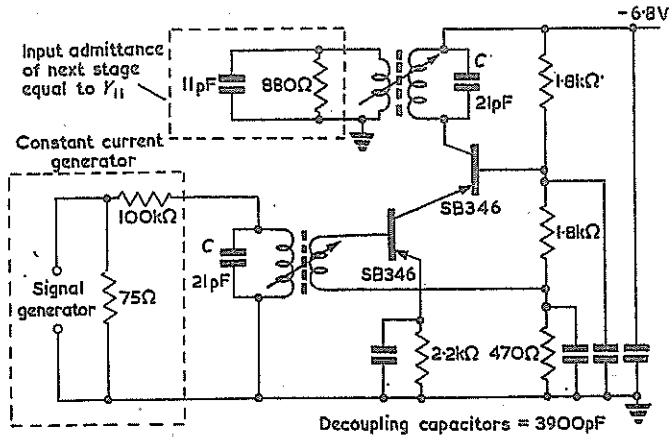

Fig. 3. Circuit diagram of experimental cascode amplifier

The Design of a Cascode Amplifier with $2G_L = G_{22}$

The circuit is similar to that in Fig. 3.

Design Details

Centre frequency 20Mc/s
Bandwidth per tuned circuit 2Mc/s
Overall bandwidth (2 tuned circuits) ..... 1·3Mc/s
Transformer ratio ..... 3·75:1
Unloaded Q (Q_U) 18
Loaded Q (Q_L) 10
Added capacitance (C) 11pF
Loss per coil ..... 7·1dB

Using 33 s.w.g. enamelled wire and tunable ferrite cup cores, the primary winding was 15 turns and the secondary 4 turns.

Results of Measurements

The input transformer tuned correctly but the output transformer most certainly showed signs of negative capacitance and resistance. The Q of the coil had increased from 10 to 14 and the value of negative resistance was calculated to be about 25kΩ with a negative capacitance of about 2pF. Allowance for the increase in the output impedance was made in the gain measurement.

Overall bandwidth ..... 1·1Mc/s
Overall gain ..... 12·9dB
Overall gain of the cascode amplifier without losses ..... 27·1dB
Maximum gain of grounded emitter amplifier .... 14·3dB

The difference in gain of 12·8dB is 3·8dB in excess of

the predicted figure. This is not surprising since in the theoretical estimation it was assumed that the feedback term was negligible.

The Design of a Cascode Amplifier with $G_L \ll G_{22}$

The circuit is similar to that in Fig. 3 except that no extra capacitance C was added to the transformers. The Q's of the coils were made very high and G_L was equal to 0·02 millimhos.

Results of Measurements

Any attempt to tune the amplifier resulted in oscillation. The circuit was taken no further.

Conclusions

The analysis has been reasonably substantiated by the practical results. Using SBT346 transistors at 20Mc/s, the experiment shows that it is possible to design a cascode amplifier (G_L slightly less than G_{22}) with unilateral properties, and 25 per cent less gain in dB than two stages of conventional neutralized grounded emitter amplification.

Numerous reports of the cascode circuit suggest the general rule, that a cascode circuit designed with any type of transistor will provide unilateral characteristics in exchange for about 25 per cent less gain in dB than two stages of grounded emitter amplification at the same frequency.

In assessing costs it should be noted that the cascode circuit has four resistors, three capacitors and one transformer less than the conventional two stage grounded emitter amplifier. Therefore all in all the cascoded amplifier may cost about the same as a conventional type.

It is believed that the cascode amplifier gives more gain for a given volume and weight, than any other transistor configuration.

Acknowledgments

The author is indebted to the Management of Semiconductors Limited for permission to publish this article.

It is believed that the transistorized cascode circuit was first used by S. H. Bowers of S.R.D.E., Christchurch.

Appendix

Derivation of Transistor Parameters in Matrix Form

Because a transistor is an active network, four terminal network theory is used in transistor c.w. circuit analysis.

A four terminal active or passive network is completely defined by equation (1).

$$\left.\begin{aligned} V_1 &= AV_2 - BI_2 \\ I_1 &= CV_2 - DI_2 \end{aligned}\right\} \quad \ldots\ldots\ldots\ldots\ldots (1)$$

A, B, C and D are constants of the network, V_1, I_1 and V_2, I_2 are the input and output voltages and currents. Equation (1) is often written in matrix notation as shown in (2).

$$\begin{vmatrix} V_1 \\ I_1 \end{vmatrix} = \begin{vmatrix} A & B \\ C & D \end{vmatrix} \begin{vmatrix} V_2 \\ -I_2 \end{vmatrix} \quad \ldots\ldots\ldots (2)$$

The array of constants is referred to as (A) or the A matrix of the network. Note that if the network is passive $[A]$ is equal to unity and in that case $AD - BC = 1$.

Equation (1) could have been written as follows (3) and in matrix form (4)

$$\left.\begin{aligned} I_1 &= Y_{11}V_1 + Y_{12}V_2 \\ I_2 &= Y_{21}V_1 + Y_{22}V_2 \end{aligned}\right\} \quad \ldots\ldots\ldots\ldots\ldots (3)$$

$$\begin{vmatrix} I_1 \\ I_2 \end{vmatrix} = \begin{vmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{vmatrix} \begin{vmatrix} V_1 \\ V_2 \end{vmatrix} \quad \ldots\ldots (4)$$

Here the Y terms are all constants whose dimensions are those of mhos and are therefore called admittance parameters. The array of Y parameters is referred to as (Y) or the Y matrix of the network. Note that if the network is passive $Y_{12} = Y_{21}$.

The relationships between Y and A parameters is as follows:

$$\left.\begin{aligned} Y_{11} &= (D/B) & Y_{12} &= \frac{-\{AD - BC\}}{B} \\ Y_{21} &= -(1/B) & Y_{22} &= (A/B) \end{aligned}\right\} \quad \ldots (5)$$

There are six ways of writing equation (1) to produce six interdependent matrices. Once any one matrix has been measured, the others can be calculated.

In practice the Y parameters are easiest to measure. Equation (3) can be re-arranged as follows to indicate the method of measurement.

$$\left.\begin{aligned} Y_{11} &= (I_1/V_1)|_{V_2=0} & Y_{12} &= (I_1/V_2)|_{V_1=0} \\ Y_{21} &= (I_2/V_1)|_{V_2=0} & Y_{22} &= (I_2/V_2)|_{V_1=0} \end{aligned}\right\} \quad \ldots\ldots (6)$$

Each measurement requires a pair of terminals of the network to be shorted out and this can be easily performed with large capacitors. Measurements can be made on an admittance bridge. connected as a two terminal device for Y_{11} and Y_{22}. and as a three terminal device for Y_{12} and Y_{21}. It will be found that some Y parameters are common for two different configurations. For example. as mentioned earlier Y_{22} (grounded emitter) is equal to y_{22} (grounded base).

Use of Matrix Algebra

Matrix Algebra is a very powerful tool when applied to transistor c.w. circuits. The following deals only with the portion used in the text.

Fig. 4 shows how two cascaded networks can be resolved into one. Writing the matrix form for the networks in full:

$$\begin{vmatrix} V_1 \\ I_1 \end{vmatrix} = \begin{vmatrix} A & B \\ C & D \end{vmatrix} \begin{vmatrix} V_2 \\ -I_2 \end{vmatrix} \text{ and } \begin{vmatrix} V_2 \\ I_2 \end{vmatrix} = \begin{vmatrix} a & b \\ c & d \end{vmatrix} \begin{vmatrix} V_3 \\ -I_3 \end{vmatrix}$$

As $-I_2 = I_2$:

$$\begin{vmatrix} V_1 \\ I_1 \end{vmatrix} = \begin{vmatrix} A & B \\ C & D \end{vmatrix} \begin{vmatrix} a & b \\ c & d \end{vmatrix} \begin{vmatrix} V_3 \\ -I_3 \end{vmatrix} = |A'| \begin{vmatrix} V_3 \\ -I_3 \end{vmatrix}$$

Using matrix multiplication:

$$|A'| = \begin{vmatrix} Aa + Bc & Ab + Bd \\ Ca + Dc & Cb + Dd \end{vmatrix}$$

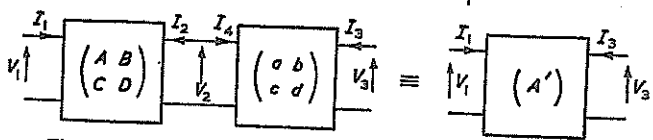

Fig. 4. The reduction of cascaded four-terminal networks

For details of the theory of matrix algebra see Aitken[2] and Bell and Brewster[3] as regards application to transistor circuit analysis.

Calculation of Transistor Performance from its Parameters

Once any set of transistor parameters is known, the performance can be assessed. Here only the use of the Y parameters will be considered. It can be shown that the maximum matched gain of a unilateralized grounded emitter amplifier, where n is the transformer ratio and shunt neutralizing is used, is as follows:

$$10 \log \left\{ \frac{|Y_{21} - Y_{12}|^2}{4\{Y_{11} - Y_{12}n\}\{Y_{22} - (Y_{12}/n)\}} \right\} \quad \ldots\ldots (7)$$

In practice Y_{12} can be neglected, at least as regards the gain calculation. There is also a power loss due to the finite Q of the unloaded coil and sometimes a mismatch

load admittance y_L. The gain equation then becomes:

$$10 \log \frac{|Y_{21}|^2}{4Y_{11}Y_{22}} - \left\{ 10 \log \left\{ \frac{1}{1 - (Q_L/Q_U)} \right\}^2 + 10 \log \frac{\{y_L + Y_{22}\}^2}{4y_L Y_{22}} \right\} \quad \ldots\ldots\ldots (8)$$

Q_L = loaded Q of the coil

Q_U = unloaded Q of the coil

As the amplifier is tuned one is only concerned with the real parts of Y_{11}, Y_{22} and y_L.

The term unilateralized implies that the input and output terminals are not coupled in the reverse direction, at any frequency. Neutralization employs less components but only causes Y_{12} to be zero over a narrow band of frequencies centred at the operating frequency. The admittance of the neutralizing network is equal to $-Y_{12}n$ (which is usually resolved into a series resistor and capacitor) and is fed from the transformer secondary.

A designer must know the design centre of Y_{12} for the transistor in use. If fixed component neutralizing is to be used, the maximum difference ΔC between the fixed capacitor and the actual series capacitance component of $-(1/Y_{12}n)$ that is likely to occur in a large batch of transistors, is calculated.

Next, the extra capacitance ΔC_0 which, when added to the fixed capacitor on a correctly neutralized amplifier will cause the stage to oscillate, is calculated from circuit details.

Once ΔC and ΔC_0 have been determined the effects of extreme misneutralization can be assessed. The stability factor S is defined as:

$$S = \frac{\text{Loop gain required for oscillation}}{\text{Actual loop gain}}$$

$$= Re \left\{ \frac{1}{\text{Actual loop gain}} \right\}$$

Or in terms of misneutralization:

$$S \simeq (\Delta C_0 / \Delta C)$$

As S becomes smaller so the interaction between the tuned circuits increases. The bandwidth becomes narrower and the peak is pulled to one side. A stability factor as low as four may be met in practice, dependent of course on the application for the amplifier. The product of the power gain and stability factor is optimum at a certain collector current.

For more details of the above, see Wolfendale[4].

REFERENCES

1. Shea, R. F. Transistor Circuit Engineering. (J. Wiley & Sons, 1957).
2. Aitken, A. C. Determinants and Matrices. (Oliver and Boyd, 1958.)
3. Bell, J. S. Brewster, K. An Introduction to Matrices and their Use in Transistor Circuit Analysis. *Electronic Engng. 31*, 98 (1959).
4. Wolfendale, E. The Junction Transistor and Its Application. (Heywood & Co. Ltd., 1958.)

AUTOMATIC CABLE TESTING

The De Havilland cable test set provides, in easily portable form, the facilities for checking the continuity and insulation of multi-core cable looms normally available only in fixed or cumbersome equipment. Although initially designed for checking electrical systems in aircraft, the unit, which weighs only 19lb is of value in any type of installation where cabling is already in place, or where the cable runs are in confined spaces.

Either a continuity or an insulation check can be carried out from one end of a cable run, the far end being terminated by a small unit weighing less than ½lb. A test is initiated by a press-button and the instrument automatically selects each wire in turn. The identification of the core undergoing test is indicated in a window which is illuminated by a red light if failure occurs, in which case the selector stops at the faulty core. Successful completion of a test sequence is indicated by the extinguishing of a separate indicator lamp.

The outlet capacity of the unit is 25 cores but this can be extended by the use of adaptors.

A single outlet from the test set can be adapted for use with any cable by means of a suitable coupler supplied against the customer's requirements. In the case of a connector having a multi-position keyway (e.g. Plessev Mk. IV) the coding is checked by a clearly marked movable keyway on both the coupler and termination units.

A high impedance source of 500V is used for the insulation tests and this provided by a transistor convertor. The continuity tests are made with a 960c/s square wave which provides 120mA on short-circuit.

The cable testers are normally supplied with fail limits set at 5Ω and 1MΩ on continuity and insulation respectively.

To enable long cable runs to be tested in conditions where the termination unit is more conveniently attached by a second operator, an intercommunication amplifier is incorporated in the instrument, connexion being made via the cable under test. Standard service style headsets may be used.

When this system is in use the operators receive an additional audible signal as each test is made and can distinguish when a cable failure is detected.

In its portable form the cable tester is mounted on a strap which can conveniently be used either as a neck-sling or a carrying-handle. Power is supplied by a lightweight battery of a type having no free electrolyte, and of sufficient capacity for about sixteen hours of normal use. Couplers and termination units can be carried in pouch-belts. For difficult situations, where access to the cable to be tested is limited, an extension cable can be used.

A charging unit can be supplied with the test set. Internal regulation of the unit ensures that in four hours the battery will be fully charged, yet there is no risk of overcharging however long the equipment is left. State of charge is indicated by a meter: an a.c. power unit is available as a replacement for the battery when the test set is in use on the bench or near a mains supply.

The portable cable tester