A MECHANICAL MODEL FOR EROSION IN COPPER CHEMICAL-MECHANICAL POLISHING

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ABSTRACT

The Chemical-mechanical polishing (CMP) process is now widely employed in the ultra-large-scale integrated semiconductor fabrication. Due to the continuous decrease in the sub-micron feature size, characterization of erosion has become an important issue in Cu CMP. In this paper, the erosion in Cu CMP is considered at two levels: wafer and die levels. Erosion models are developed based on the material removal rates, Cu interconnect area fraction, linewidth and Cu deposit thickness. Experiments have been conducted to obtain the selectivity values among Cu, barrier layer and dielectric, and wafer-level material removal rate ratio for validating the new erosion model. The present model is compared with the existing models and is found to better agree with the experimental data.

I. INTRODUCTION

Continuing advances in ultra-large-scale integration technology require the fabrication of submicron-size features of higher resolution, denser packing and multi-layer interconnects. Recently, copper has emerged as the optimal interconnect material because of its low electrical resistivity and resistance to electromigration. Patterned Cu lines are produced by a damascene scheme, comprising oxide trench patterning and Cu deposition, followed by chemical-mechanical polishing (CMP). The current success in producing high resolution interconnects is due to the excellent local and global planarization capabilities of the Cu CMP process.

Fig. 1 schematically shows a single layer Cu interconnect structure before and after CMP. A diffusion-barrier layer and Cu are deposited in the etched dielectric trenches as shown in Fig. 1(a). Then the Cu CMP process is employed to remove excess Cu and the barrier layer without excessive loss of interconnect lines and the dielectric. It has been reported in the literature that the material removal rate in the Cu CMP process is related to the local pattern geometry and material being polished [1-5]. Although the ideal Cu CMP process finishes polishing the excess Cu and barrier layer at the same time over the entire wafer, as shown in Fig. 1(b), there often exists non-uniformity in the real case, as shown in Fig. 1(c), due to different material removal rates for each layer and the underlying pattern geometry. Since the end-point of the Cu CMP process requires that the excess Cu and barrier layer are removed completely there are overpolished dielectric areas, resulting in erosion. Moreover, because the soft interconnect Cu is polished faster than the hard dielectric material, the Cu line is dished as shown in Fig. 1(c).

Erosion and dishing in Cu CMP reduce the thickness of both dielectric and Cu interconnects and results in surface non-planarity, which can significantly affect the chip performance. Thus, the mechanisms of erosion and dishing must be determined and their impact on process yield addressed. Erosion and dishing problems in Cu CMP have been addressed in recent studies [2, 3]. It has been reported that erosion is more significant than dishing in the small Cu interconnect linewidth regions, such as the device level features, and that dishing is more important than erosion in the large Cu linewidth region of top layers of a multi-level damascene structure. The continuous advances in semiconductor fabrication technology and decreasing sub-micron feature size make it more important to characterize erosion in Cu CMP. Due to the complexity of material removal by mechanical, chemical and chemomechanical interactions in the CMP process, the mechanisms of erosion and the effects of pattern geometry and material properties in Cu CMP process are still not fully explored.

In this study, a systematic way of characterizing erosion in Cu CMP is presented. A model based on the local pressure distribution, to focus on the mechanical aspects of the polishing process, is suggested. Moreover, a theoretical framework for relating wafer-level and die-level erosion to process parameters is established.

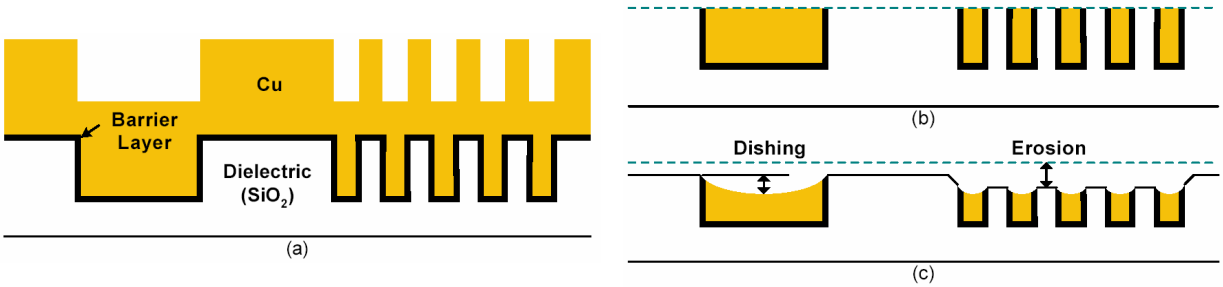

Fig. 1. Schematics of a single layer Cu interconnect: (a) before polishing (b) ideal case after polishing and (c) real case after polishing.

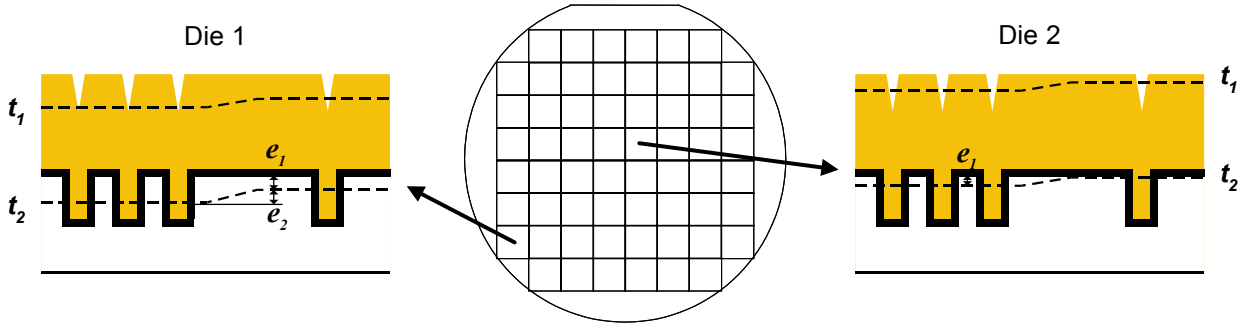

Fig. 2. Evolution of a polishing surface at two different dies in a wafer during CMP process, which accounts for wafer-level erosion, e_1, and die-level erosion, e_2. Material removal rate in die 1 is higher than that in die 2.

II. THEORY

A. Definition of erosion

In general, each point on a wafer has a different material removal rate due to different chemical effects, pressure, relative velocity, slurry transportation, and initial topography. Because the end-point of the Cu CMP process should be the time when all of the excess copper and barrier layer are completely removed, there are always overpolished regions. Erosion in Cu CMP is defined as the amount of overpolished dielectric thickness with respect to the original dielectric film thickness as shown in Fig. 2.

Fig. 2 shows time evolution of the surface being polished at two different dies on a wafer during the Cu CMP process. The material removal difference causes non-uniformities at two levels: wafer-level and die-level. To characterize wafer-level non-uniformity, two points, which are located in different dies but have the same feature pattern geometries are considered. When a certain feature of same pattern geometry on Die 1 and Die 2 are compared, Die 1 will always be polished faster than Die 2 because of its higher material removal rate. To characterize die-level non-uniformity, two different feature pattern geometries in the same die are considered. After polishing for a certain time, two different features on a die will have different material removal rates. Generally, a feature with a large area fraction of Cu interconnect lines will be polished faster than a feature with a small area fraction.

In this study, based on the schematics in Fig. 2, wafer and die-level erosion are defined as e_1 and e_2, respectively. e_1 is defined as the amount of overpolishing of a local reference point of the original dielectric with respect to a global reference point. The local reference point can be any point which has same pattern feature in each die and the global reference point is the slowest polishing point in a wafer. e_2 is defined as the dielectric layer thickness difference with respect to each local reference point, which is mainly dependent on the pattern geometry. The blanket area in each die is considered as a local reference point.

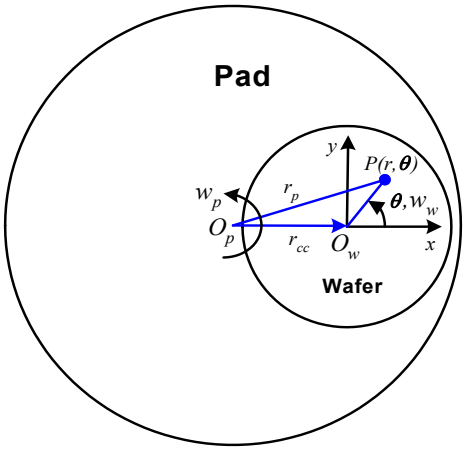

Fig. 3. Schematic of the coordinate system for a rotary CMP process

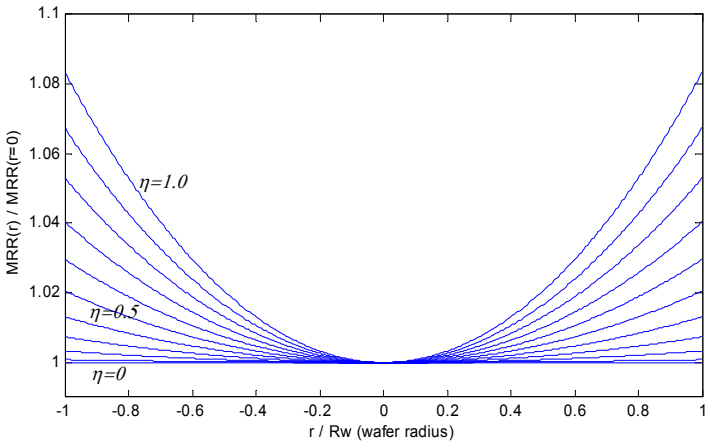

Fig. 4. Material removal rate ratio distribution for various η, where $\eta \equiv (\omega_w - \omega_p)/\omega_p$.

B. Effect of relative velocity

To consider the kinematics of the Cu CMP process, a coordinate system for a rotary polisher is shown in Fig. 3. The rotational centers of the platen and the wafer are O_p and O_w, and the angular velocities are ω_p and ω_w, respectively. The two rotational axes are normal to the polishing plane with an offset r_{cc}. The relative velocity, $v_R(r,\theta)$, at point $P(r,\theta)$ in the wafer can be expressed as:

$$v_R(r,\theta) = \sqrt{\omega_p^2 r_{cc}^2 + (\omega_p - \omega_w)^2 r^2 + 2\omega_p(\omega_p - \omega_w) r_{cc} r \cos\theta} \quad (1)$$

$$v_R(\rho,\theta) = v_R(0)\sqrt{1 + (\rho\eta)^2 + 2(\rho\eta)\cos\theta} \quad (2)$$

where, $v_R(0,\theta) = v_R(0) = \omega_p r_{cc}$, $\rho \equiv r/r_{cc}$ and $\eta \equiv (\omega_p - \omega_w)/\omega_p$. The material removal rate (MRR) at each point on the wafer may be calculated by the Preston equation [6] and compared with that of the center.

$$MRR = \left|\frac{dh}{dt}\right|(\rho,\theta) = k_p \cdot p \cdot v_R(\rho,\theta) \quad (3)$$

Thus, the material removal ratio between a point $P(r)$ and that at the center of the wafer is

$$\frac{\Delta h(\rho)}{\Delta h(0)} = \frac{1}{2\pi}\int_0^{2\pi} \sqrt{1 + (\rho\eta)^2 + 2(\rho\eta)\cos\theta}\, d\theta \quad (4)$$

Fig. 4 shows the variation of the material removal ratio in the wafer for different η. When $\eta = 0$ $(\omega_p = \omega_w)$, the wafer-level non-uniformity is zero. Although the wafer-level non-uniformity increases as η increases, the effect of this variation is small. For example, even when the angular velocity of the wafer is 50% greater or less than that of the platen $(\eta = 0.5)$, the variation of wafer level non-uniformity is only 2%. Thus the direct effect of the relative velocity variation on the wafer-level non-uniformity is not a significant factor in the CMP process.

C. Basic material removal rate prediction scheme

Fig. 5 shows the basic terms for general material removal rate prediction in the Cu CMP process. Although the Preston equation represents a local material removal rate, it is often used as an average material removal rate on the wafer level in blanket wafer polishing. In that case, the Preston constant, pressure and relative velocity are considered as uniform over the entire wafer. Thus, a new dimensionless term χ is introduced as the the normalized material removal rate of a blanket wafer.

$$\chi \equiv k_p \cdot p_{av} \quad (5)$$

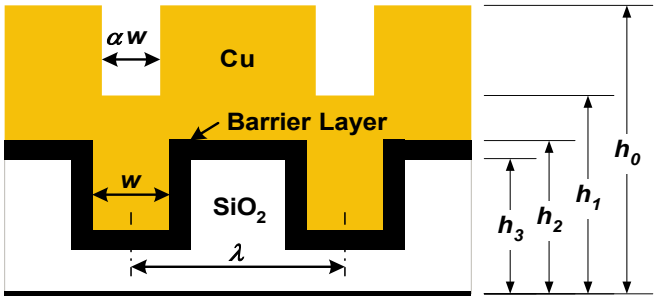

Fig. 5. Definition of basic terms used in the erosion model.

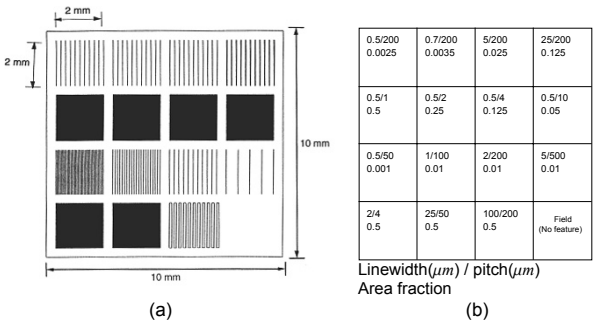

Fig. 6. Schematics of the CMP mask: (a) mask layout and (b) pattern geometry layout

Pattern geometry can be represented by two parameters: area fraction, A_f, and linewidth, w, of Cu interconnect lines. Although the underlying pattern geometry of Cu damascene structure can be represented by A_f and w, there is another factor which must be included. Due to the characteristics of the Cu deposition process, such as physical vapor deposition (PVD) and electroplating, the deposited Cu pattern is quite different from the original mask pattern. It is observed that the Cu pattern linewidth is smaller than the original Cu interconnect linewidth in the PVD Cu patterned wafer, and that the ratio of these two linewidths is mainly dependent on the original Cu interconnect linewidth. To characterize this ratio, α is defined as:

$$\alpha \equiv \frac{w_{up}}{w_{original}}, \quad w_{up} = \alpha\, w_{original} \quad (0 \le \alpha \le 1) \tag{6}$$

Now, the parameter β is introduced to express the wafer-level non-uniformity in the erosion model, which represents the material removal ratio between two points having the same pattern geometry on different dies in a wafer.

$$\beta \equiv \frac{|\frac{dh}{dt}|_{die1}}{|\frac{dh}{dt}|_{die2}} = \frac{\chi_{die1}}{\chi_{die2}} \quad (0 \le \beta \le 1) \tag{7}$$

Another factor to be considered is the local pressure distribution parameter, γ, which is defined as the ratio of Cu interconnect line pressure, p_{Cu}, and average pressure, p_{av}. When polishing starts, the pad contacts the top surface of a wafer. At this stage, the value of γ can be set to zero because the deposited pattern line is empty and the pad deformation is restricted. As the pattern is polished, the whole wafer surface starts holding pressure and the γ value is changed to one. As the pad contacts the barrier layer, γ value starts decreasing from one to zero since the material removal rates of the barrier layer or the dielectric region and the Cu interconnect are different.

$$\gamma \equiv \frac{p_{Cu}}{p_{av}} \quad (0 \le \gamma \le 1) \tag{8}$$

The material removal rate at each height stage in Fig. 5 can be expressed based on the local pressure distribution as:

$$\begin{aligned} h_0 < h < h_1 \quad & \left|\frac{dh}{dt}\right| = \frac{\chi_{Cu} v_R}{1-\alpha A_f} & h_2 < h < h_3 \quad & \left|\frac{dh}{dt}\right| = \chi_b v_R \left(\frac{1-\gamma A_f}{1-A_f}\right) \\ h_1 < h < h_2 \quad & \left|\frac{dh}{dt}\right| = \chi_{Cu} v_R & h_3 < h < h_4 \quad & \left|\frac{dh}{dt}\right| = \chi_{ox} v_R \left(\frac{1-\gamma A_f}{1-A_f}\right) \end{aligned} \tag{9}$$

D. Wafer level erosion

Fig. 7 shows the schematic for a time-based erosion calculation model.

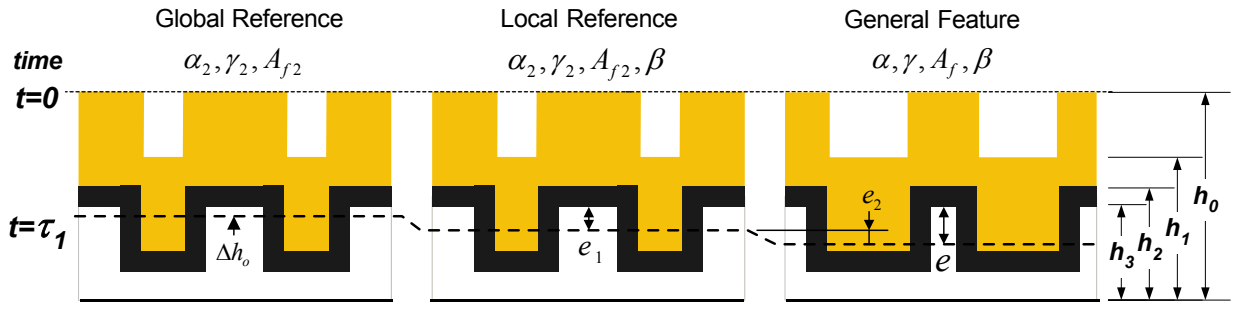

Fig. 7. Schematics of time-based erosion, e, calculation for general feature with respect to the global and local reference points when a global reference point is overpolished in the amount of Δh_o. Wafer-level erosion, e_1, and die-level erosion, e_2, are calculated separately.

$\tau_{1,global}$ is defined as the time when the global reference point finishes polishing, and $\tau_{1,local}$ and $\tau_{1,general}$ are the time intervals calculated in terms of local reference point and general feature point.

$$\tau_{1,global} = \frac{h_0 - h_1}{\chi_{Cu} v_R \left(\frac{1}{1-\alpha_2 A_{f_2}}\right)} + \frac{h_1 - h_2}{\chi_{Cu} v_R} + \frac{h_2 - h_3}{\chi_b v_R \left(\frac{1-\gamma_2 A_{f_2}}{1-A_{f_2}}\right)} + \frac{\Delta h_o}{\chi_{ox} v_R \left(\frac{1-\gamma_2 A_{f_2}}{1-A_{f_2}}\right)} \tag{10}$$

$$\tau_{1,local} = \beta \left[\frac{h_0 - h_1}{\chi_{Cu} v_R \left(\frac{1}{1-\alpha_2 A_{f_2}}\right)} + \frac{h_1 - h_2}{\chi_{Cu} v_R} + \frac{h_2 - h_3}{\chi_b v_R \left(\frac{1-\gamma_2 A_{f_2}}{1-A_{f_2}}\right)} + \frac{e_1}{\chi_{ox} v_R \left(\frac{1-\gamma_2 A_{f_2}}{1-A_{f_2}}\right)} \right] \tag{11}$$

$$\tau_{1,general} = \beta \left[\frac{h_0 - h_1}{\chi_{Cu} v_R \left(\frac{1}{1-\alpha A_f}\right)} + \frac{h_1 - h_2}{\chi_{Cu} v_R} + \frac{h_2 - h_3}{\chi_b v_R \left(\frac{1-\gamma A_f}{1-A_f}\right)} + \frac{e}{\chi_{ox} v_R \left(\frac{1-\gamma A_f}{1-A_f}\right)} \right] \tag{12}$$

By comparing τ_1 in the global reference point and local reference point, the wafer-level erosion e_1 can be expressed as:

$$e_1 = \left(\frac{1}{\beta} - 1\right) \left[\frac{\chi_{ox}}{\chi_{Cu}} \left(\frac{1-\gamma_2 A_{f_2}}{1-A_{f_2}}\right) \left[(1-\alpha_2 A_{f_2})(h_0 - h_1) + (h_1 - h_2) \right] + \frac{\chi_{ox}}{\chi_b}(h_2 - h_3) \right] + \frac{1}{\beta}\Delta h_o \tag{13}$$

To consider the wafer-level erosion specifically, a local reference point for each die needs to be selected in order for the pattern effect to be disregarded. In this study, a test mask set has 15 different pattern features and 1 field (no pattern) region per each die as shown in Fig. 6. The field region with no feature is chosen as a local reference point for the erosion model. Thus, wafer-level erosion e_1 for the local reference points for each die can be rewritten as:

$$e_1 = \left(\frac{1}{\beta} - 1\right) \left[\frac{\chi_{ox}}{\chi_{Cu}}(h_0 - h_2) + \frac{\chi_{ox}}{\chi_b}(h_2 - h_3) \right] + \frac{1}{\beta}\Delta h_o \tag{14}$$

Eq. 14 shows that three parameters significantly contribute wafer-level erosion. One is the wafer-level non-uniformity factor β, the other is the blanket normalized material removal rate ratios among Cu, barrier layer and the dielectric, and the third is the amount of overpolishing, Δh_o, of the global reference point.

E. Die level erosion

By comparing the time τ_1 between the local reference point and a general feature point, the total erosion e can be expressed as:

TABLE I

EXPERIMENTAL CONDITIONS

Parameters	Value
Diameter of Wafer (mm)	100
Normal Load (N)	391
Normal Pressure (kPa)	48
Rotational Speed (rad/s)	7.8
Linear Velocity (m/s)	0.70
Duration (s)	60-360
Slurry Flow Rate (ml/s)	2.5

TABLE II

BLANKET MATERIAL REMOVAL RATE

Abrasive Material		Al_2O_3	Al_2O_3	SiO_2	CeO_2
Particle Size (nm)		1000	300	1000	1000
Coating materials	Cu	489	213	372	49
	Ta	27	13	128	149
	TaN	25	12	72	74
	SiO_2	34	14	383	123

MRR Unit = nm/min

$$e = \frac{\chi_{ox}}{\chi_{Cu}}\left(\frac{1-\gamma A_f}{1-A_f}\right)(\alpha A_f - \alpha_2 A_{f_2})(h_0-h_1) + \frac{\chi_{ox}}{\chi_b}\left[\left(\frac{1-\gamma A_f}{1-A_f}\right)\left(\frac{1-A_{f_2}}{1-\gamma_2 A_{f_2}}\right)-1\right](h_2-h_3) + e_1\left(\frac{1-\gamma A_f}{1-A_f}\right)\left(\frac{1-A_{f_2}}{1-\gamma_2 A_{f_2}}\right) \quad (15)$$

The die-level erosion e_2 can be defined as the difference between the total erosion, e, and the wafer-level erosion, e_1, or $e_2 = e - e_1$. Again, the same local reference point from the wafer-level erosion calculation, which is blanket area of each die, will be needed to be able to separate the die-level erosion from wafer-level erosion. Thus, e_2 is defined as the relative oxide thickness of each feature in a die with respect to the oxide thickness of the local reference point in the same die.

$$e_2 = \left(\frac{A_f}{1-A_f}\right)\left[\frac{\chi_{ox}}{\chi_{Cu}}(1-\gamma A_f)\alpha(h_0-h_1) + \frac{\chi_{ox}}{\chi_b}(1-\gamma)(h_2-h_3)\right] + \left(\frac{A_f}{1-A_f}\right)(1-\gamma)e_1 \quad (16)$$

Eq. 16 shows that several parameters affect the amount of the die-level erosion in Cu CMP, such as the area fraction of a feature A_f, the local pressure distribution factor γ, the interconnect deposition factor α and the blanket material removal rates of the Cu, barrier layer and dielectric, χ_{Cu}, χ_b and χ_{ox}. Also, wafer-level erosion affects die-level erosion.

III. EXPERIMENTS

Experiments were conducted on a rotary CMP machine under the conditions listed in Table. I. The normal pressure was 48 kPa, and the relative velocity was maintained at 0.7 m/s over the wafer by setting the rotational velocity of the wafer and the platen the same. The polishing duration was varied from 1 to 6 min to determine the blanket material removal rates of Cu, oxide and diffusion barrier layer.

IV. RESULTS

A. Blanket material removal rate

The developed wafer and die-level erosion models show that one of the major factors that affect erosion is selectivity, the ratios of blanket material removal rates among Cu, dielectric and the barrier layer. Therefore, it is necessary to get the blanket material rate of each material for different slurries. Four different slurries were used for three different blanket material coatings and the results are listed in Table. II.

B. Cu interconnect line deposition factor α and the wafer-level non-uniformity factor β

The interconnect deposition factor α was determined by imaging the deposited top surface of a patterned wafer by Scanning Electron Microscopy (SEM). Fig. 8 shows the results of the SEM measurement of two points with the same area fraction (0.5) and different linewidths (0.5 μm and 2 μm). PVD Cu patterned

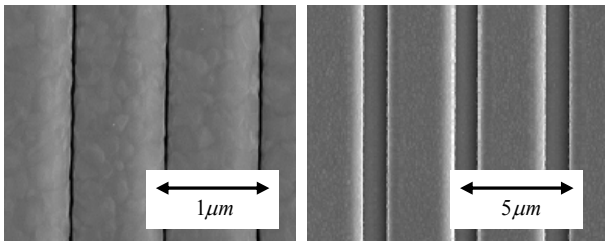

Fig. 8. SEM micrographs for determining the interconnect deposition factor, α, (a) $A_f = 0.5, w = 0.5\mu m, \alpha = 0.1$ and (b) $A_f = 0.5, w = 2\mu m, \alpha = 0.8$.

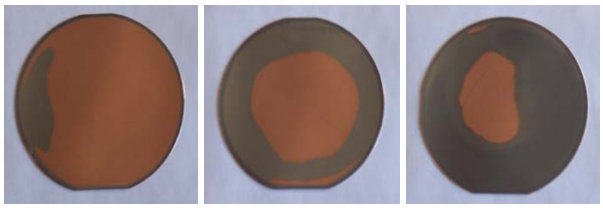

Fig. 9. The effect of wafer-level non-uniformity factor, β in Cu blanket wafer polishing at (a) t=2min, (b) t=3min and (c) t=4min.

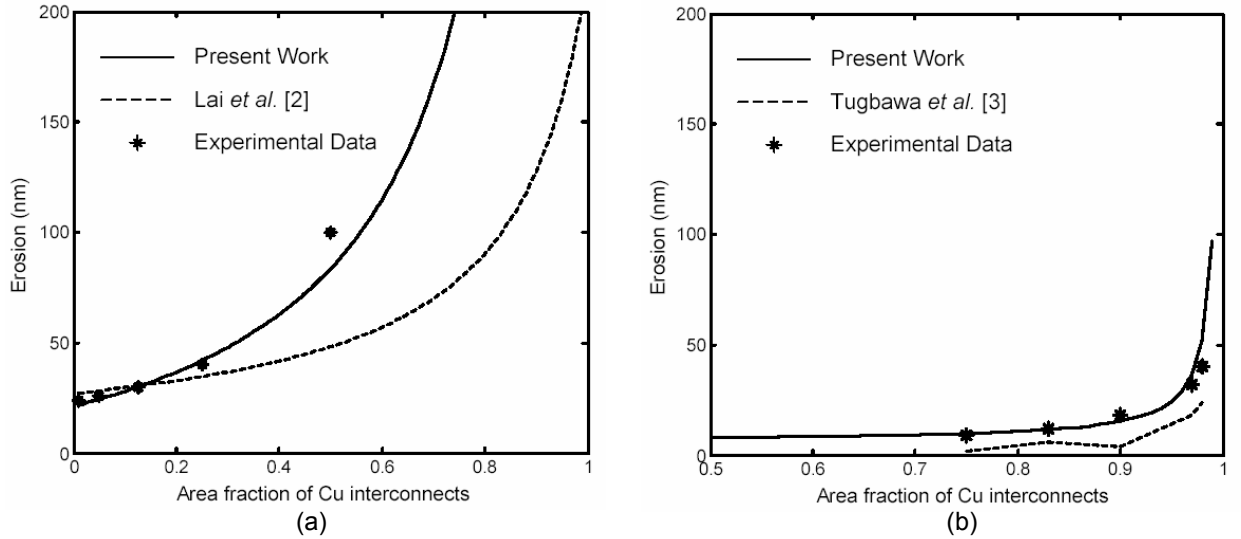

Fig. 10. Model verification for experimental results and comparison with the model of (a) Lai *et al.* [2]: mainly addressed for small A_f and (b) Tugbawa *et al.* [3]: mainly addressed for large A_f.

wafers were used for SEM measurements. The results show that the value of α is closely related to the Cu interconnect linewidth w. If the linewidth is greater than 5 μm, α is about 0.9, which means that the deposited pattern reflects the original mask pattern very well. If the linewidth is smaller than 1 μm, α is under 0.1 and the top surface could be considered as blanket area. In the range between these two ($1\mu m < w < 5\mu m$), α increases with the linewidth w.

The wafer-level non-uniformity factor β was quantified by the material removal rate of blanket wafer at two different points on the wafer. Fig. 9 shows the Cu blanket wafers after 2 min, 3 min and 4 min of polishing time during CMP process. The figure shows that the edge of the wafer is being polished faster than the center area as polishing time increases, and that the maximum ratio of material removal rate is close to 0.8. Each CMP machine, however, can have different β values.

C. Model verification

After all the parameter values from the previous section such as selectivity, α and β are determined, these values were used for calculating the amount of wafer-level and die-level erosion based on the proposed model. Two different sets of previous data were used to verify the present erosion model. Fig. 10(a) shows the experimental data and an erosion model by Lai *et al.* [2] and the present model. The present model agrees with the experimental data more closely in the middle and small values of area fraction than the Lai *et al.* model. These data show that the present erosion model can predict the erosion well in the less packed pattern geometry with the area fraction under 0.5.

Fig. 10(b) shows the data and an erosion model by Tugbawa *et al.* [3] and the present model. Most of

the data in these experiments are from the densely packed region with an area fraction over 0.7. The present model still matches the experimental data well.

V. CONCLUSIONS

Both analytical and experimental studies on the erosion in the Cu CMP process are presented in this paper and the following conclusions are drawn.

1. The erosion of Cu damascene structure is defined by the thinning of oxide feature with respect to the original oxide thickness. To identify the sources of erosion systematically, wafer-level and die-level erosion are defined separately. The possible sources of erosion at each level are identified, such as Cu interconnect deposition factor α, wafer-level non-uniformity factor β, local pressure distribution factor γ and blanket wafer normalized material removal rate, χ. Redefining erosion as wafer-level and die-level makes it possible to identify the sources of erosion and their effects more clearly.

2. Based on the kinematics of a rotary CMP machine, the material removal rate ratio distribution for various angular velocities of wafer and platen was described. It is shown that a direct effect of the relative velocity variation on the wafer-level non-uniformity is not significant in the CMP process.

3. A basic material removal rate calculation scheme was developed by using the local pressure distribution. Pattern geometries for each stage were defined by the area fraction, A_f, linewidth, w, of the Cu interconnects and the local pressure was calculated at each height stage. Other local effects during polishing were included in the normalized blanket material removal rate.

4. Experiments were conducted to determine the values of each parameter. The blanket wafer material removal rates for each material layer were determined for different types of slurries. For a given mask pattern geometry, the Cu interconnect deposition factor α was measured by SEM and it is shown that α is strongly related to Cu linewidth and deposition method. The wafer-level non-uniformity factor β was also determined by the blanket Cu wafer polishing experiments.

5. The developed erosion model was compared with the existing erosion models and experimental data. The proposed model agrees well with the erosion data both in the low area fraction region ($A_f < 0.5$) and in the packed interconnect region ($A_f > 0.5$).

ACKNOWLEDGMENT

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