Microsystems Technology Laboratories

The Microsystems Technology Laboratories (MTL) is an interdepartmental laboratory that operates with the mission to foster research and education in semiconductor process and device technology, as well as in integrated circuits and systems design. MTL provides micro- and nanofabrication and computer-aided design (CAD) infrastructure to the entire campus. The laboratory has 35 core faculty members who are engaged in diverse research areas related to electronic device fabrication, integrated circuits and systems, photonics, micro-electro-mechanical systems (MEMS), and molecular and nanotechnologies. The most recent addition to MTL's core membership is senior research scientist Luis Velasquez. In addition, 110 affiliate faculty and senior research staff benefit from the fabrication facilities and CAD infrastructure provided by MTL. During AY2011, more than 700 researchers, primarily graduate students, conducted research using MTL's advanced infrastructure, and MTL recovered approximately 77 percent of operating expenses through charges to users and underwrote the remaining balance through unrestricted funds (approximately $1.1M). Sponsored programs administered directly through MTL have an annual research volume of approximately $15M.

MTL's fabrication environment includes three clean rooms, totaling 7,800 square feet: the 6-inch capable class-10 Integrated Circuits Laboratory, the class-100 Technology Research Laboratory, and the flexible Exploratory Materials Laboratory. The computational environment provides access to advanced electronic design automation for device, circuit, and system design. The fabrication and computation facilities are maintained and operated by approximately 20 full-time technical staff members.

MTL engages users in a number of technical events and hosts a regular seminar series spanning diverse technical areas related to devices and circuits. A committee, chaired by professor Tomas Palacios, organizes the series, which is open to the public. In addition, MTL hosts occasional distinguished seminars. The MTL annual research conference (MARC) is run by MTL graduate students in collaboration with a steering committee, chaired by professor Jing Kong. MARC is widely attended by industry, faculty, students, and staff and provides a unique opportunity to learn about research in the diverse areas encompassed by MTL, while helping to encourage interaction among the MTL community. The 2011 conference was held at the Cambridge Marriott hotel and attracted 240 attendees. MTL also held the third workshop on next-generation medical electronics, a two-day event held on campus that featured talks from leading experts and a lively poster session. On December 2–3, 2010, MTL and the MIT Energy Initiative co-hosted the workshop Next Generation μ-Energy Systems, with professor Anantha Chandrakasan as event chair.

MTL partners with industry through the Microsystems Industrial Group (MIG), and its research and operation are significantly subsidized by the MIG consortium. MIG donates major pieces of equipment to MTL, contributes directed fellowships, and provides access to state-of-the-art integrated circuit chip fabrication services. This year, Hitachi Hi-Tech, Murata Manufacturing, and Maxim Integrated Products joined MIG. Members of MIG's industrial advisory board provide significant guidance in shaping the vision of MTL.

Research conducted at MTL can be broadly classified into the following categories: circuits and systems, electronic devices, energy, materials, medical electronics, MEMS and BioMEMS, nanotechnology, and photonics. MTL has four affiliated research centers with focused themes: the Center for Integrated Circuits and Systems, MEMS@MIT, the Center for Graphene Devices and Systems, and the Center for Integrated Photonics Systems.

Administration, Management, and Operations

Professor Chandrakasan is the MTL director and oversees the daily administration and management of the laboratory. Three faculty associate directors—professors Jesús del Alamo, Judy Hoyt, and Hae-Seung "Harry" Lee—assist the director in managing the computational and fabrication infrastructure, as well as the communications and sponsor relations aspects of MTL, respectively. Two staff associate directors provide direct support for the fabrication facilities (Vicky Diadiuk) and the administrative services, compliance, and industry liaisons (Samuel Crooks).

MTL maintains several committees charged with policy development and implementation, including the policy board (Professor Chandrakasan, chair), process technology committee (Dr. Diadiuk, chair), and computation committee (Professor del Alamo, chair). MTL also has a social committee (personnel administrator Debroah Hodges-Pabon, chair) that aims to build community spirit among its many users, and a publications committee (media specialist Mara Karapetian, chair) working on MTL's annual research report and annual newsletter, Micronotes. MTL community members are also involved in other functional committees.

Shared Service Facilities

MTL's microfabrication, testing, and computational facilities are open to the entire MIT community, as well as to researchers from other universities and government laboratories through the MTL outreach programs. Similarly, the Fabrication Facilities Access Program enables local industrial access to the clean room facilities.

MTL has committed significant resources to the acquisition and maintenance of capital equipment. These capital improvements, upgrades, and purchases allow MTL to serve an increasingly diverse user base. Many MIG member companies donate capital equipment that is used in the fabrication and computation facilities.

Fabrication Facilities

MTL's fabrication resources are managed and operated by a group of professional technical staff. All researchers planning to utilize MTL fabrication facilities are required to successfully complete a safety and orientation course before use and must receive training from a research specialist for each piece of laboratory equipment they plan to operate. The facilities support research on projects involving a range of substrates, including silicon, germanium, III–V semiconductors, organics, and glass; they include capabilities for deposition of a wide range of materials, such as dielectrics, plastics, semiconductors, metals, carbon nanotubes, and graphene. The process technology committee includes students, faculty, and staff and meets weekly to review user process flows, in addition to requests for new materials, protocols, and fabrication operational issues.

Computation Facilities

MTL also maintains a comprehensive computation infrastructure, providing a broad array of services to the community. MTL supports the CAD tools required for circuit and system design. Seamlessly connected to the computation infrastructure is MTL's common object representation for advanced laboratories (CORAL), through which users of MTL's fabrication facilities interface with the fabrication tools to perform their processes. The user log is coupled to a charging algorithm that calculates user fees on a monthly basis. CORAL was developed in collaboration with Stanford University and continues to evolve as the needs of MIT's microfabrication community require.

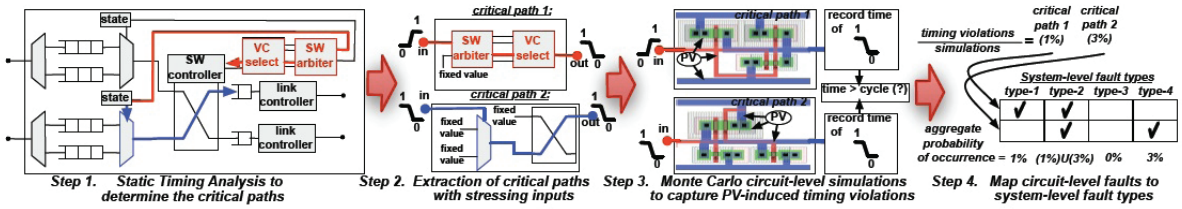
During AY2011, MTL supported 704 registered users, of which 26 were faculty and 45 were technical, research, and administrative staff. The remaining 633 were active users of MTL's microfabrication, computational, and CAD service facilities.

Research Highlights

Enabling System-level Modeling of Variation-induced Faults in Networks-on-chip: K. Aisopos, O. Chen, and L.-S. Peh

Process variation is increasingly threatening the reliability of networks-on-chips, the critical communication fabric in many-core chips. Thus, various resilient router designs have been recently proposed and evaluated. However, these evaluations assume random fault distributions, which result in 52–81 percent inaccuracy. Professor Peh's group proposes an accurate circuit-level fault-modeling tool that can plug into any system-level NoC simulator, quantify the system-level impact of process variation–induced faults at runtime, pinpoint fault-prone router components that should be protected, and accurately evaluate alternative resilient multi-core designs.

K. Aisopos, O. Chen, and L.-S. Peh. 2011. Enabling System-level Modeling of Variation-induced Faults in Networks-on-chip. 48th Design Automation Conference. San Diego, CA.

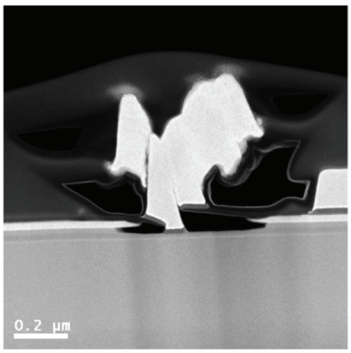


Proposed NoC fault model methodology.

Self-aligned InGaAs High-electron Mobility Transistor with Outstanding Frequency Response: J. del Alamo

In this research, a new self-aligned gate technology has been developed for InGaAs high-electron mobility transistors (HEMTs) to reduce parasitic resistance and eventually the footprint of the device. The new approach uses non-alloyed Mo ohmic contacts and a very low parasitic capacitance gate design, and delivers an extremely small contact resistance and an unprecedented source resistance. The ohmic contacts also exhibit

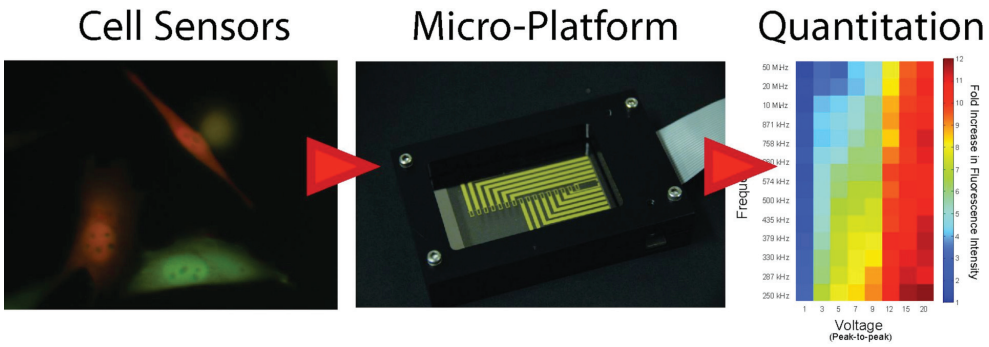
excellent thermal stability. Using this technology, a 60 nm gate length self-aligned InGaAs HEMT has been demonstrated with world-record high-frequency characteristics for this gate length, strongly suggesting a path towards obtaining field-effect transistors capable of operating in the 1 THz regime.



Cross section of 60 nm gate length self-aligned InGaAs High-Electron Mobility Transistor. The distance between the ohmic contact and the edge of the gate is about 100 nm.

Cell-based Sensors for Quantifying the Physiological Impact of Microsystems: S. Desai and J. Voldman

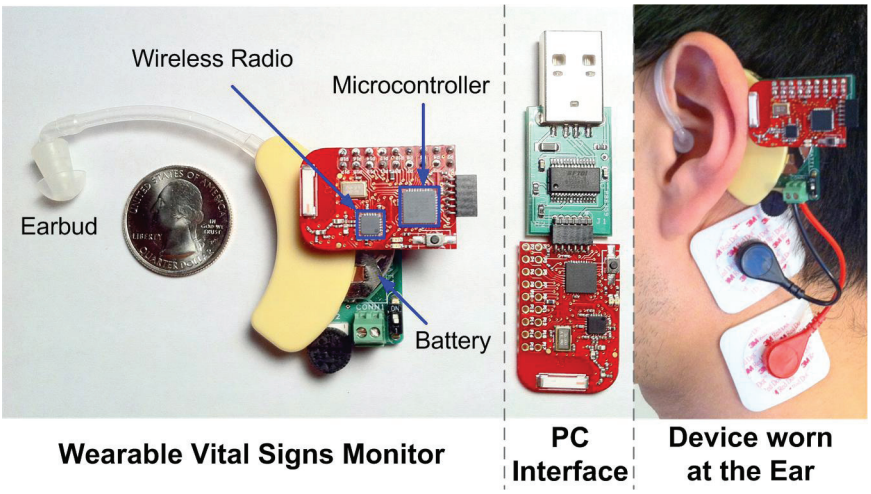
Microsystems are increasingly used in the manipulation, patterning, and sorting of cells. Critical to the widespread adoption of these new technologies is an understanding of their impact on cellular physiology. In this research, a system was recently developed that integrates a cell-based sensor, a microfabricated electrical screening platform, and quantitative imaging to enable the first large-scale physiological screens of the impact of microsystems on cells (*Integrative Biology*, 2011). To perform physiological screening, a cell-based sensor was developed that expresses a green fluorescent protein when the cell is stressed. The integration of this quantitative physiological sensor with a microfabricated system enabled the execution of multiplexed screens across >140 electric field variations on >200,000 cells. This is the first time such detailed and comprehensive maps of the impact of a microsystem stressor on cell phenotype have been created. These maps will guide designers in the development of cell-innocuous systems and users in the proper use of such systems to minimize impacts.



Cell-based sensors for determining physiological impact of microsystems. The left panel shows fluorescence-readout based cell sensors which when coupled with an electric-field-screening microsystem (middle panel) can be used to quantitatively determine (right panel) the physiological impact of electric fields in microsystems. Such cell-based sensors could be applied to myriad microsystems to better understand the stresses imposed on living mammalian cells in microscale platforms.

A Wearable Vital Signs Monitor at the Ear: D. He, E. Winokur, and C. Sodini

Cardiovascular disease affects 37 percent of the population and is the leading cause of death in the United States. Vital signs monitors aid the early detection of cardiovascular diseases by providing the long-term data necessary for an accurate and timely diagnosis. In this research, the site behind the ear is proposed as a location for an integrated wearable vital signs monitor that continuously measures heart rate, blood pressure, blood oxygenation, cardiac output, and respiratory rate. The device is designed to use the ear as a discreet and natural anchor that reduces device visibility and the need for skin adhesives. This location offers physiological signals such as the electrocardiogram (ECG), the photoplethysmogram (PPG), and the head ballistocardiogram (hBCG). The ECG measures the electrical activity from the heart and yields information such as continuous heart rate, blood pressure (when coupled with PPG), and respiratory rate. The PPG measures the blood volume and color under the skin using optical illumination and gives information such as continuous heart rate and blood oxygenation. The hBCG measures the head's mechanical reaction to the blood expelled by the heart and offers information about continuous heart rate and cardiac output.

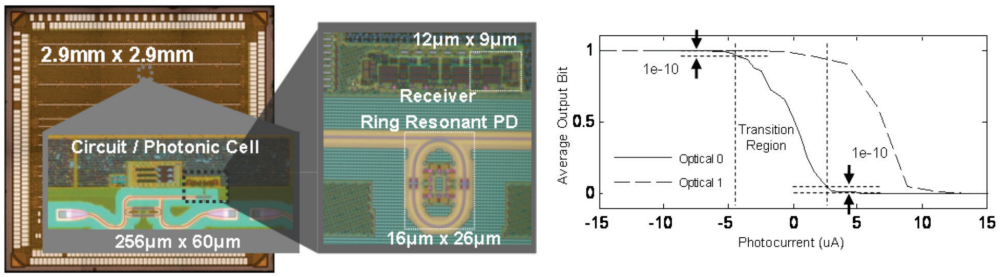


The wearable vital signs monitor, the PC USB interface, and the monitor being worn at the ear with ECG electrodes attached.

Monolithically Integrated Optical Interconnects in 45 nm CMOS SOI: V. Stojanovic and R. Ram

In this research, a breakthrough design and integration methodology was developed that incorporates silicon-photonic components (waveguides, couplers, modulators, and photodetectors) into the front end of the advanced sub-100 nm complimentary metal-oxide-semiconductor (CMOS) and CMOS silicon on insulator (SOI) processes, with no process changes. This integration has the potential to transform the high-volume very large-scale integration semiconductor industry, ranging from processor and application-specific integration circuit manufacturers to dynamic random-access memory makers, enabling high-bandwidth, low-energy on-chip, and chip-to-chip communication. Illustrated is the first example of a silicon-photonic component (a silicon germanium photodetector) monolithically integrated with a high-energy efficiency electrical receiver. This monolithic integration also enables in-situ characterization of devices/

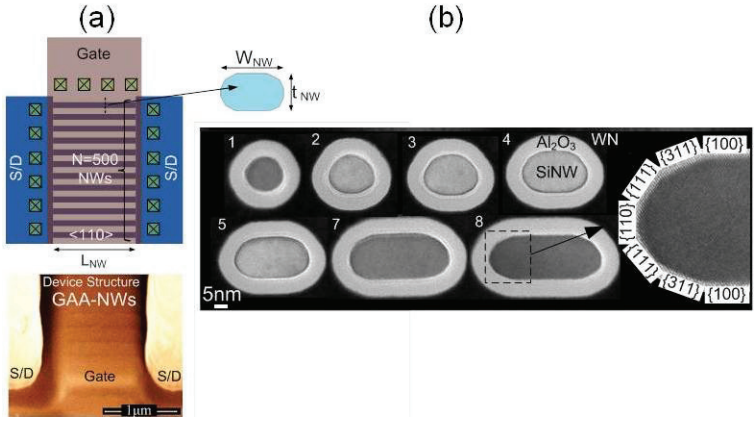
circuits. The receiver is characterized in-situ and shown to operate with uA-sensitivity at 3.5 Gbps with a record low power consumption of 180µW (52 fJ/bit) and area of 108µm2.



EOS electronic-photonic integration platform die photo. Inset shows a circuit/photonic characterization test-cell with integrated receiver and resonant photo-detector. The "logic 1" and "logic 0" values as a function of the photo-current sensed at the receiver are shown on the right.

Silicon Nanowire MOSFETs with High-k/Metal Gate Technology: P. Hashemi, J. Teherani, and J. Hoyt

The scalability of conventional planar silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) is limited by the ability of the gate to control the drain current at sub-10 nm gate lengths. Silicon nanowire channel MOSFETs are of great interest for this application because the gate-all-around geometry improves the ability of the gate to turn off transistor current at very short gate lengths. "Top-down" fabricated nanowires are compatible with existing CMOS processes; however, the lithography and etch processes leave rough sidewalls that degrade carrier mobility. Professor Hoyt's group has been studying the transport of electrons and holes in nanowire channel MOSFETs and recently demonstrated gate-all-around devices with conformal, high-k dielectric/metal gate technology, and nanowire diameters as small as 10 nm. In a paper published at the 2010 International Electron Devices Meeting, a high temperature hydrogen annealing process was shown to reshape and smooth the nanowires, improving the hole mobility. These results are promising for the ultimate scalability of CMOS technology.



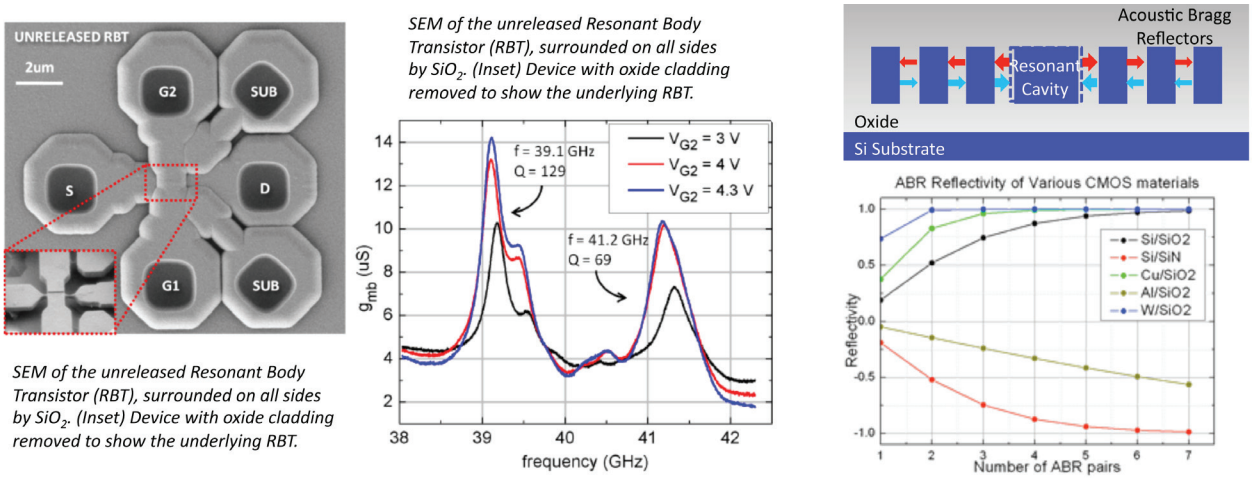
Views of the fabricated gate-all-around Si nanowire MOSFETs: (a) (top) schematic device structure and (bottom) colorized scanning electron microscope image of completed device, and (b) transmission electron micrographs of the nanowire cross sections showing various shaped Si nanowires that were studied, and the conformal Al2O3 gate dielectric.

HybridMEMS Lab: D. Weinstein

The HybridMEMS Lab, led by professor Dana Weinstein, is working to develop innovative micro-electro-mechanical devices and systems for low-power, compact wireless communication, physical sensors, and timing applications. The lab focuses on new mechanical designs and efficient transducers to make MEMS resonators with high resonance frequency, low motional impedance, strong transducer coupling coefficient, low bias drift, and wide programmable range. Over the past year, significant progress has been made toward unreleased MEMS resonators operating at radio frequency (RF) and mm-wave frequencies, which can be fabricated at front-end-of-line processing in CMOS with no post-processing or costly packaging. Specifically, the group has demonstrated the first fully-unreleased acoustic resonator: a silicon-based independent gate FinFET surrounded on all sides by SiO2. This FinFET–MEMS device, operating at 39 GHz (quality factor [Q] of 129), was presented at the 2011 Institute of Electrical and Electronics Engineers (IEEE) International Conference on MEMS, marking the highest acoustic frequency in Si to date, with f.Q products comparable to released devices at octaves lower frequency [1]. The design and optimization of acoustic Bragg reflectors was performed to maximize quality factor in unreleased resonators, and was shown to significantly suppress spurious resonant modes while providing resonator Q's comparable to their released counterparts [2]. Investigation of fundamental limits of this technology and exploration into device optimization, integration, and control will provide circuit designers with basic building blocks for RF and mm-wave applications, including wireless communication, high-accuracy frequency sources for timing applications and navigation, and integrated temperature sensing in CMOS.

[1] W. Wang, L. Popa, R. Marathe, and D. Weinstein. 2011. An unreleased mm-wave resonant body transistor. IEEE International Conference on Micro Electro Mechanical Systems (MEMS 2011), 1341–44. Cancun, Mexico.

[2] W. Wang and D. Weinstein. 2011. Acoustic Bragg reflectors for Q-enhancement of unreleased MEMS resonators. IEEE Frequency Control Symposium (FCS 2011). San Francisco, CA.

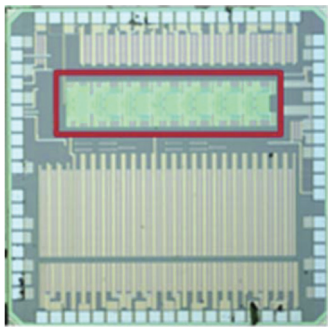


(left) Experimental measurement of first unreleased Si bar resonator with quality factor of 129 at 39 GHz. (right) Both quality factor and suppression of undesired modes can be improved by orders of magnitude using acoustic Bragg reflectors surrounding the resonator body. Very few layers are necessary to obtain almost perfect acoustic reflection using materials commonly found in the CMOS stack.

Voltage Scalable Analog Circuits: S. Lee, H.-S. Lee, and A. Chandrakasan

Power supply voltage scaling is a powerful technique to reduce power consumption of digital circuits. The non-linear relation between the power consumption and speed is exploited by varying the power supply voltage with the speed demand of the circuit. In most electronic systems, analog circuits are an integral part of the system. Power supply voltage scaling has not been successful in analog circuits for primarily three reasons: 1) typical analog circuits employing operational amplifiers require large power supply voltages and hence do not tolerate lower voltages than the nominal power supply voltages very well, 2) maintaining gain and stability of the operational amplifier is extremely challenging over wide range of speed and power supply voltages, and 3) analog circuits need to provide certain signal-to-noise ratio. At lower power supply voltages, the signal range is smaller and maintaining the signal-to-noise ratio becomes more difficult. For these reasons, conventional voltage scalable analog circuits exhibit poor power efficiency, which defeats the purpose.

In this research, revolutionary zero-crossing based circuits are employed for power supply voltage scalable analog circuits. This class of circuits provides the advantages of operational amplifier-based circuits without their gain and stability issues. Moreover, these circuits are more than an order of magnitude power efficient and can operate at much lower power supply voltage, making them ideally suited for power supply voltage scaling. The first prototype of the circuits is a 12-bit pipeline analog-to-digital converter, whose power supply voltage can be varied between 0.5 and 1 volt. At the nominal 1 volt power supply, the maximum sampling rate of 50 mega samples per second is achieved with over 11 effective number of bits. The power efficiency measured by a figure of merit (FOM) is 41 fJ/step, making it the most power efficient analog-to-digital converter in its performance range. More importantly, as the power supply voltage is lowered, the FOM further improves without sacrificing the effective number of bits. At 0.5 volt, the achieved FOM is 28 fJ/step. The die photograph of the prototype built in a standard 65 nm digital CMOS technology is shown in Figure 8.



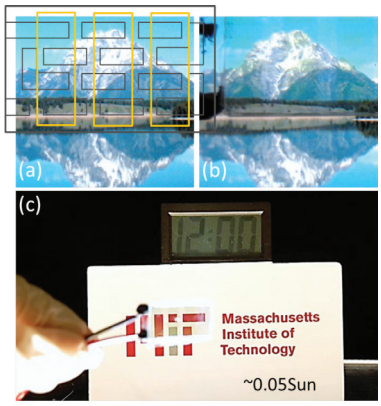
Voltage Scalable Analog-to-Digital Converter in 65 nm CMOS.

Transparent Organic Photovoltaics for Window Applications: R. Lunt and V. Bulovic

The low-energy density of solar illumination necessitates deployment of solar technologies over large surface areas in order to capture enough of the sun's energy to offset a significant portion of non-renewable energy consumption. The obstacle of large-area deployment could be overcome with development of a low-cost, transparent, photovoltaic (PV) technology that can be integrated onto window panes in homes, skyscrapers, and automobiles, enhancing the functionality of already utilized transparent surfaces. Since glass, structural framing, and inverters comprise nearly 40 percent of thin-film PV module prices, integrating solar cells into windows can also reduce effective installation costs. Previous efforts to construct semitransparent devices have focused on the use of thin active layers (or spatially segmented films) with light absorption focused in the visible spectrum,

and therefore have been limited to either low efficiencies or low average visible-light transmissivity, since both parameters cannot be simultaneously optimized.

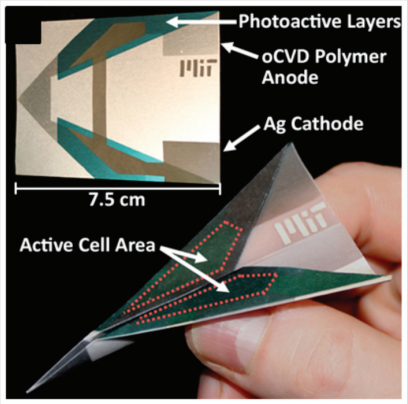
In this work, an additive transparent organic PV technology is demonstrated that can similarly retain the glass transparency, where the non-transmitted light in the near-infrared is utilized for power generation. The excitonic character of organic and molecular semiconductors is exploited to produce PV architectures with structured absorption, i.e., exhibiting minima and maxima that are uniquely distinct from the band-absorption of their inorganic counterparts. Combining these PVs with selective high-reflectivity near-infrared mirrors, a prototype transparent device is demonstrated with a power conversion efficiency of several percent, while also permitting more than 60 percent transmission of visible light through the entire device. The work also demonstrates that a series-integrated array of these transparent cells is capable of powering electronic devices under near-ambient lighting, making them useful for distributed and point-of-source utilization of solar energy.

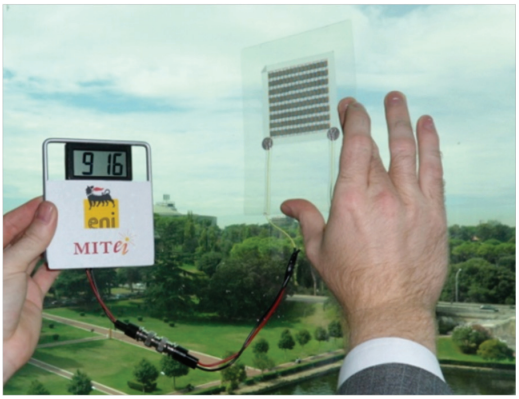


(a-b) Picture of the "Teton mountains" with the fully assembled transparent solar cell in front of the picture where the cell design is shown in (a). (c) Picture of the series-integrated transparent organic soar cell (positioned in front of the MIT logo) powering an LCD clock.

Paper-thin and Paper-based Organic Photovoltaics: R. Lunt, M. Barr, J. Rowehl, K. Gleason, and V. Bulovic

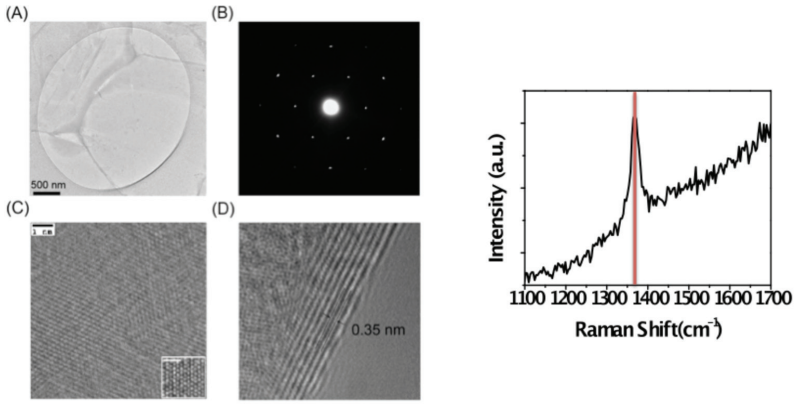
There is emerging interest in the ability to produce low-cost and lightweight solar cells and other electronics on flexible, stretchable, and foldable substrates. Rigid glass or silicon substrates in the current designs represent a large fraction of the overall module cost and also restrict how and where modules can be deployed. Thus, a shift to the design of modules specifically on low-cost substrates could open untapped locations for solar deployment, including formats that are ubiquitous in society (e.g., textiles, window curtains, printed paper documents, and wallpaper). PV devices fabricated directly on common fiber-based paper substrates are also foldable and rollable for storage and portability, easily shaped for three-dimensional applications, and able to be stapled to the roof structures or glued onto walls. To this end, there is significant interest in integrating various electronics to low-cost paper substrates, including transistors, storage devices, and displays. In this research, the use of oxidative chemical vapor deposition is examined in conjunction with organic PVs to fabricate PV cells directly on fiber-based and paper substrates that are both flexible and foldable. For example, in the left image below, a paper PV cell is shown that was folded into a paper airplane (see corresponding video here. Furthermore, paper-based, monolithically series-integrated arrays have been designed that are capable of powering common electronics, such as small-format liquid crystal (LCD) displays under ambient light as shown in the image on the right, with shelf lifetimes greater than several months. These demonstrations allow the rethinking of how and where lightweight and potentially low-cost PVs can be deployed.





Synthesis and Transfer of Large-area, Few-layer Hexagonal Boron Nitride Films: K. Kim and J. Kong

Hexagonal boron nitride (*h*BN) is a III-V compound with structures very similar to graphite and has been referred to as "white graphite." It is also a layered structure material with weak van der Waals interaction between the layers. Within each layer, its honeycomb structure is composed of alternating boron and nitrogen atoms instead of all carbon atoms, as in graphene. While graphene or graphite is metallic or semi-metallic in terms of the electrical property, *h*BN is an insulator with a direct wide-band gap (5.97 eV). The in-plane mechanical strength and thermal conductivity of *h*BN has been reported to be about the same as those of graphene, whereas *h*BN has even higher chemical stability than grapheme—it can be stable in air up to 1000°C (in contrast, for graphene the temperature is ~600°C). Similar to graphene, *h*BN has a wide range of applications based on its remarkable properties. Recently, it is reported that the on-substrate mobility of graphene on exfoliated single crystalline *h*BN is comparable to that of suspended graphene due to its ultra-flat and charge impurity-free surface. Giant flexoelectric effect was also predicted for monolayer *h*BN, which suggests *h*BN's potential for ambient agitation energy harvesting. The group has developed a chemical vapor deposition synthesis technique to obtain single- or few-layer *h*BN films on metallic substrate. Similar to the graphene film, these *h*BN films can be transferred to various substrates. The group is currently characterizing *h*BN film structure and properties and integrating it into graphene transistor devices.



MEMS **Embedded**

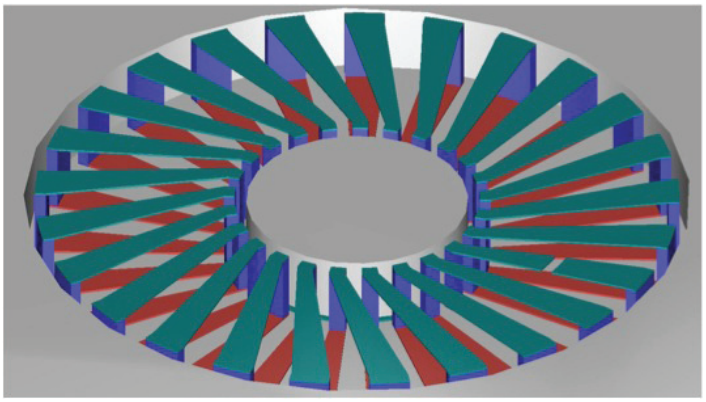
(left): Transmission Electron Microscope images of the hBN film. (right): Raman spectrum of hBN film.

Inductors: J. Lang

Passive components—namely inductors, transformers, and capacitors—are often the largest and most expensive components in power electronic circuits, and the magnetic components (inductors and transformers) are often responsible for a large portion of power loss. As operating frequencies are increased, the physical size of the passive components can, in theory, be correspondingly reduced while maintaining or improving efficiency. However, increases in frequency also increase the severity of several losses. Realizing the potential for miniaturization and ultra-high efficiency requires new magnetic component designs, fabrication strategies, and materials.

As the switching frequencies of the power electronics rise and the size of the magnetics fall, new fabrication strategies for the magnetics become possible. In particular, with sufficiently small volume the magnetics can be embedded in the substrate of the power circuit or within a secondary substrate and flip-bonded above the power circuit. Moreover, toroidal magnetics fabricated in this manner provide the self-shielding necessary to mitigate electromagnetic interference, and they can be fabricated using standard MEMS bulk fabrication processes.

PhD student Mohammad Araghchini and professor Jeffrey Lang have developed designs for embedded inductors and transformers that enable high-frequency operation and realize small size and low loss. Their work focuses on toroidal magnetics, such as that shown schematically in Figure 12. It is anticipated that all conductors in the figure will be fabricated from electroplated copper. The figure suggests that the inductor is buried in the power electronics chip itself. Fabrication within a separate insulating substrate is also under study.



A toroidal inductor buried within an integrated-power-electronics chip.

Awards and Honors for Core Faculty

Sang-Gook Kim received the Department of Mechanical Engineering Joseph H. Keenan Award for Innovation in Undergraduate Education for his efforts in the development of Course 2.674: Micro/Nano Engineering Laboratory. The award recognizes outstanding educators who have made innovations in the educational paradigm, in either curriculum content or methodology.

Sung Jae Kim received the Technology Idol award at the 2011 Global Water Summit (Germany). He was also awarded the 2010 grand prize at the Hyundai Engineering and Construction thesis competition (South Korea).

Lih Feng Cheow received the Research Laboratory of Electronics 2011 Helen Carr Peake Research Prize.

Hae-Seung "Harry" Lee was named the inaugural holder of the Department of Electrical Engineering and Computer Science advanced television and signal processing chair.

Judy Hoyt was co-recipient—with MTL affiliate faculty member Eugene Fitzgerald—of the 2011 IEEE Andrew S. Grove Award. The annual award is presented to an individual for "outstanding contributions to solid-state devices and technology."

Affirmative Action

MTL supports the affirmative action goals of the Institute.

Anantha P. Chandrakasan
Director
Professor of Electrical Engineering and Computer Science