Microsystems Technology Laboratories

The MIT Microsystems Technology Laboratories (MTL) is an interdepartmental laboratory with a mission to foster research and education in semiconductor process and device technology and in integrated circuits and systems design. MTL provides micro- and nanofabrication and computer-aided design (CAD) infrastructure to the entire campus. MTL has 32 core faculty members who are engaged in diverse research areas related to electronic device fabrication, integrated circuits and systems, photonics, microelectromechanical systems (MEMS), and molecular and nanotechnologies. In addition, 81 affiliate faculty and senior research staff benefit from the fabrication facilities and CAD infrastructure provided by MTL. Last year, more than 550 researchers, primarily graduate students, conducted research using the MTL infrastructure. MTL recovers approximately 75% of operating expense through charges to users and underwrites the remaining balance through use of unrestricted funds (approximately $1 million for FY2008). Sponsored programs administered directly through MTL have an annual research volume of approximately $15 million.

MTL's fabrication environment includes three clean rooms totaling 7,800 square feet: the state-of-the-art class-10 Integrated Circuits Laboratory, the class-100 Technology Research Laboratory, and the flexible Exploratory Materials Laboratory. The computational environment provides access to advanced electronic design automation for device, circuit, and system design. The fabrication and computation facilities of MTL are maintained and operated by approximately 20 full-time technical staff members.

MTL engages users in a number of technical events. MTL hosts a regular seminar series spanning diverse technical areas related to devices and circuits. A committee chaired by Professor Joel Dawson arranges the seminar series, open to the public. In addition to these regular seminars, MTL also hosts occasional distinguished seminars. Most recently, MTL (in collaboration with the Industrial Liaison Program) hosted the visit of Craig R. Barrett, chairman of the board of Intel Corporation in February 2008. MTL holds an annual research conference (MARC) run by MTL graduate students in collaboration with a steering committee chaired by Professor Joel Voldman. The conference is widely attended by industry, faculty, students, and staff (MARC 2008 attracted more than 220 attendees). MARC is a unique opportunity to learn about research in the diverse areas encompassed by MTL and helps encourage interaction among the MTL community.

MTL partners with industry through the Microsystems Industrial Group (MIG). MTL research and operation is significantly subsidized by the MIG consortium. MIG donates major pieces of equipment to MTL, contributes directed fellowships, and provides access to state-of-the-art IC chip fabrication service. This year, two new members joined MIG: ST Microelectronics and Taiwan Semiconductor Manufacturing Corporation. Members of the Industrial Advisory Board (http://www-mtl.mit.edu/mig/iab.html) provide significant guidance in shaping the vision of MTL.

Research conducted at MTL can be broadly classified into five categories: circuits and systems, electronic devices, MEMS and BioMEMS, molecular and nanotechnology, and photonics. MTL has four affiliated industrial research centers with more focused

interests: the Center for Integrated Circuits and Systems, Intelligent Transportation Research Center, MEMS@MIT, and the Center for Integrated Photonic Systems.

Administration, Management, and Operations

Professor Anantha Chandrakasan is the MTL director with oversight for daily administration and management of the lab. Two faculty associate directors, Professor Jesus del Alamo and Professor Judy Hoyt, assist the director in managing the computational and fabrication infrastructure, respectively. Two staff associate directors provide direct support for the fabrication facilities (Dr. Vicky Diadiuk) and administrative services, compliance, and industry liaison (Mr. Samuel Crooks).

MTL maintains several committees charged with policy development and implementation, including the policy board (chair: A. Chandrakasan), process technology committee (chair: V. Diadiuk), and computation committee (chair: J. del Alamo). MTL also has a social committee (chair: Debroah Hodges-Pabon) that builds community spirit among our many users and a publications committee (chair: Mara Karapetian) working on MTL's Annual Research Report (http://mtlweb.mit.edu/research/ar.html) and newsletter. MTL community members are also involved in other functional committees.

Shared Service Facilities

MTL's microfabrication, testing, and computational facilities are open to the entire MIT community as well as researchers from other universities and government laboratories through the MTL Outreach Programs. Similarly, the Fabrication Facilities Access Program enables local industrial access to the clean room facilities.

MTL has committed significant resources to the acquisition and maintenance of capital equipment. These capital improvements, upgrades, and purchases allow MTL to serve an increasingly diverse user base. Many of the MIG member companies donate capital equipment that is used in the fabrication and computation facilities.

Fabrication Facilities

MTL's fabrication resources are managed and operated by a group of professional technical staff. All researchers planning to utilize MTL fabrication facilities are required to successfully complete a safety and orientation course before use and must receive training from a research specialist for each piece of laboratory equipment they plan to operate. The facilities support research on projects involving a range of substrates including silicon, germanium, III–V semiconductors, organics, and glass; they include capabilities for deposition of a wide range of materials such as dielectrics, plastics, semiconductors, metals, and carbon nanotubes. The process technology committee includes students, faculty, and staff and meets weekly to review user process flows in addition to requests for new materials, protocols, and fabrication operational issues.

Computation Facilities

MTL also maintains a comprehensive computation infrastructure, providing a broad array of services to the community. MTL supports the CAD tools required for circuit and system design. Seamlessly connected to the computation infrastructure is MTL's

common object representation for advanced laboratories (CORAL), with which the users of MTL's fabrication facilities interface with the fab tools to perform their processes. The user log is coupled to a sophisticated charging algorithm that calculates user fees on a monthly basis. CORAL was developed in collaboration with Stanford University and continues to evolve as the needs of MIT's microfabrication community require.

Research Highlights

World Record InGaAs Field-Effect Transistor: D.-H. Kim and J. A. del Alamo

Professor del Alamo's group is investigating a new generation of transistors that are capable of extending the microelectronics roadmap for several more generations. Professor del Alamo is attempting to do this by taking advantage of the extraordinary electron transport properties of InGaAs, InAs, and other compound semiconductors.

In the last year, Dr. Dae-Hyun Kim in Professor del Alamo's group has achieved a 30-nm-long InGaAs high-electron mobility transistor (HEMT) that has displayed a world record frequency response (Figure 1). A current-gain cut-off frequency, fT, of 628 GHz has been demonstrated. fT is a closely watched figure of merit that is used to evaluate the suitability of transistors for high-frequency and high-speed operation. The value reported by del Alamo's group is the highest fT ever obtained in any field-effect transistor in any material system. This bodes well for the suitability of transistors in this material system for ultra-high-speed logic and THz applications.

Kim, D.-H., and J. A. del Alamo. 2008. 30 nm InAs pseudomorphic HEMTs on InP substrate with current-gain cutoff frequency of 628 GHz. IEEE Electron Device Letters *29(8): 830–8332008.*

Organic Solar Concentrators: M. Currie, J. Mapel, T. Heidel, S. Goffri, and M. Baldo

Photovoltaic concentrators aim to increase the electrical power obtained from solar cells (Figure

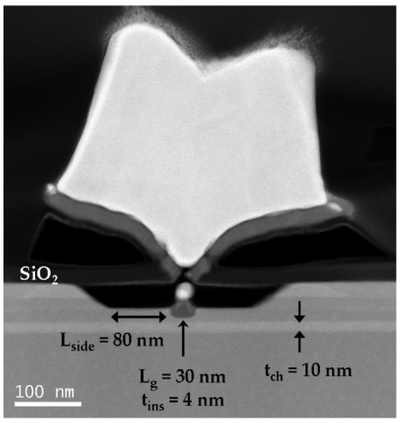

Figure 1. 30 nm InAs HEMT with record f_T.

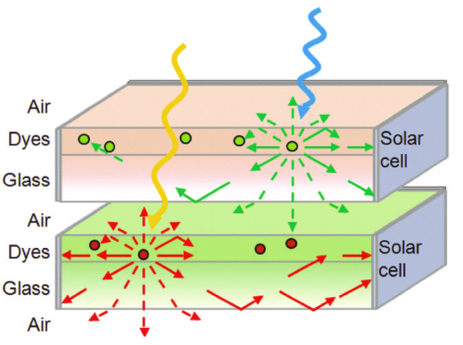

Figure 2. Physical configuration of organic solar concentrators (OSCs). OSCs consist of a thin film of organic dyes deposited on high refractive index glass substrates. Dyes absorb incident solar radiation and reemit it at a lower energy. Approximately 80% of reemitted photons are trapped within the waveguide by total internal reflection for ultimate collection by a photovoltaic device mounted on the substrate edges. Photon loss (dashed lines) occurs via nontrapped emission or absorption by other dyes. Light transmitted through the top OSC can be captured and collected by a second OSC whose dyes absorb and emit light at lower energies for electrical conversion at a second, lower bandgap PV device. Alternatively, the bottom OSC can be replaced by a low-cost PV cell or be used to heat water in a hybrid PV thermal system.

2). Conventional solar concentrators track the sun to generate high optical intensities, often by using large mobile mirrors that are expensive to deploy and maintain. We have demonstrated a large improvement in low-cost solar concentrators. Our new devices increase the power obtained from solar cells by a factor of more than 40 without needing to track the sun. These results are at least a factor of four better than previous results.

Currie, M. J., J. K. Mapel, T. D. Heidel, S. Goffri, and M. A. Baldo. 2008. High-efficiency organic solar concentrators for photovoltaics. Science *321(5886): 226–228.*

Graphoepitaxy of Block-Copolymers by Using Sub-10-nm Lithographically Defined Structures: I. Bita, J. K. Yang, Y. S. Jung, C. Ross, E. Thomas, and K. Berggren

Working with collaborators in the Department of Materials Science and Engineering (professors Ross and Thomas), we have found a way to control self-assembly using top-down engineered structures that form lithographic "surrogates" for block-copolymer microdomains (Figure 3). The result is a two-dimensional lattice of self-assembled polymer sphere structures that can be controlled explicitly through the positioning of nearby lithographic silica pillars. The final periodic structures form surprising commensurate lattices with the templating lattice, which can then be controlled through explicit control of the template positions. This work is likely to find application in single-magnetic-domain storage or in lithography for beyond-CMOS electronics manufacturing.

Bita, I., J. K. Yang, Y. S. Jung, C. A. Ross, E. L. Thomas, and K. K. Berggren. 2008. Graphoepitaxy of self-assembled block copolymers on two-dimensional periodic patterned templates. Science *321(5891): 939–943.*

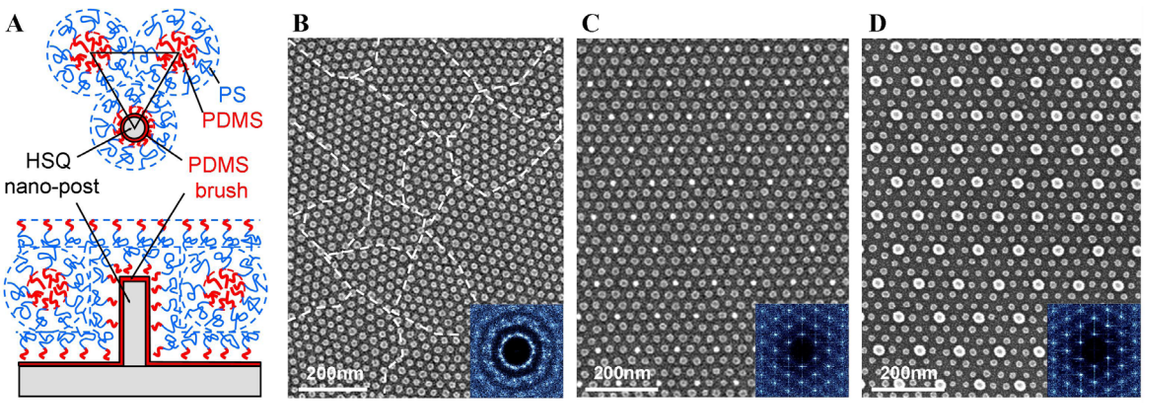

Figure 3. a. Top-down and side-view schematics showing the arrangement of PS-b-PDMS block copolymer molecules in the region surrounding a single post made from cross-linked HSQ resist. b. Scanning electron micrograph (SEM) of a disordered monolayer of BCP spherical domains formed on a flat surface, i.e. without templating. Dashed lines indicate boundaries between self-assembled grains. Insets are two-dimensional Fourier transforms of the domain positions, showing the absence of long-range order. c. d. SEM images of ordered BCP spheres formed within a sparse 2D lattice of HSQ posts (brighter dots) with different surface and post functionalizations. The BCP microdomains formed an ordered lattice with a factor of three increase in spatial frequency over that of the post lattice. Insets show the 2D Fourier transforms indicating a high degree of 2D lattice order.

A 0.3V Micropower Processor with Embedded DC-DC Converter: J. Kwong, Y. Ramadass, N. Verma, and A. Chandrakasan

Ultra-low-voltage operation can minimize the energy consumed per switching event and extend the battery lifetime of portable electronics. We have demonstrated an ultra-low-voltage microcontroller that can be powered with energy-harvesting technology. While most current chips operate at around 1 V, this microcontroller functions between 0.3 V and 0.6 V, consuming 27.2 pJ per cycle of active energy, an order of magnitude less than a comparable commercial microcontroller. It employs several specialized circuit design techniques to enable operation down to these ultra-low voltages. The logic design and verification methodology specifically target manufacturing process variation, which worsens severely at low voltages, to ensure robust operation. The memory uses an eight-transistor bit-cell and specialized peripheral circuit assists to enable aggressive voltage scaling despite the extreme variation. To practically minimize energy, however, highly efficient low-voltage power delivery to the logic and SRAM is essential. An on-chip, switched-capacitor DC-DC converter employs multiple-gain settings and low-overhead control circuitry to deliver variable load voltages and achieve >75% efficiency. We have successfully powered this chip using a thermoelectric generator and are exploring other energy-harvesting solutions. The microcontroller chip was fabricated in 65-nm CMOS by Texas Instruments (Figure 4) and was reported at the 2008 International Solid-State Circuits Conference [1].

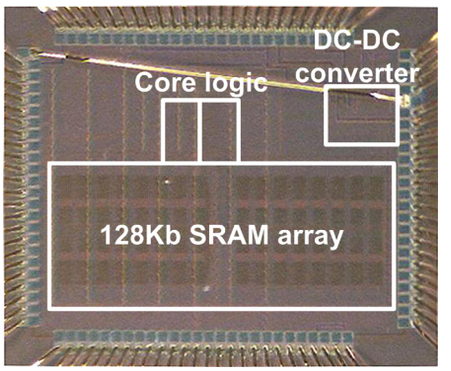

Figure 4. Die micrograph of ultra-low-voltage microcontroller chip.

Kwong, J., Y. Ramadass, N. Verma, M. Koesler, K. Huber, H. Moormann, and A. Chandrakasan. 2008. A 65nm sub-V_t microcontroller with integrated SRAM and switched-capacitor DC-DC converter. IEEE International Solid-State Circuits Conference—Digest of Technical Papers, *318–319.*

A New Architecture for Implantable Radio Frequency Transceivers: J. L. Dawson

Very recently, the Federal Communications Commission has dedicated a frequency band specifically for medical telemetry, allowing for radio frequency communications between a medical implant and a base station. Although this standard has existed for almost a decade, current solutions do little to exploit the unique features of the

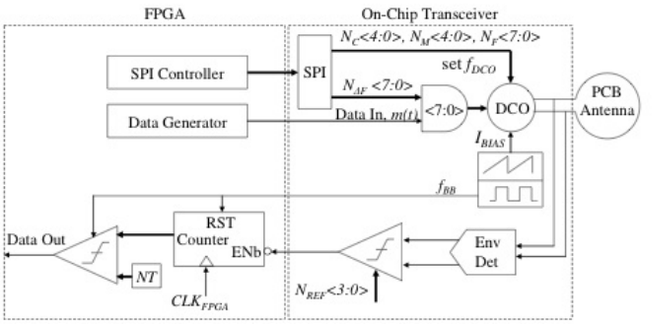

Figure 5. The new IC architecture uses a direct modulated DCO for the transmit path and a superregenerative circuit for the receive path. These choices are made possible by the temperature stability of the body and allow us to reduce both the size and the power dissipation of the IC compared with commercially available units.

implant environment to lower the cost and power dissipation as well as reduce the size of implantable transceivers.

We recently proposed a new architecture for implantable transceivers that specifically exploits the temperature stability of the implant environment. A fabricated integrated circuit (IC) in a 90-nm CMOS technology successfully illustrated the concept, and we presented a paper on it at this year's VLSI Symposium (Figure 5).

Enhancement of Immunoassays Using Concentration Devices Using Nanofluidic Protein Concentration System: Y.-C. Wang and J. Han

When the target analyte concentration is much less than the antibody-analyte binding constant KD, primary immunobinding is severely limited, and therefore prolonged immunoassay incubation time is necessary. Recently, we used a nanofluidic protein concentration system to enhance a standard bead-based immunoassay and demonstrated that both immunoassay sensitivity and detection dynamic range can be enhanced significantly [1]. With a 30-min preconcentration, we were able to enhance the immunoassay sensitivity by more than 500-fold, from 50 pM to the sub-100 fM range. This was achieved with a simulated molecular background (10 μg of green fluorescent protein per mL, nonspecific to the antibody) in the sample solution, demonstrating the possibility of detecting directly from complicated protein mixtures (Figure 6). The volume of immunosensor is only 10 to 100 pL, and even after ~10,000-fold or more preconcentration this device would not consume more than ~1 μL of the original sample volume for a single detection. This would provide unique opportunity for detecting multiple markers from precious human fluid samples (amniotic or cerebrospinal fluid) from patients. We also demonstrated that the same idea can be applied to measure low-abundance enzyme activity [2] by concentrating the enzyme and substrate together.

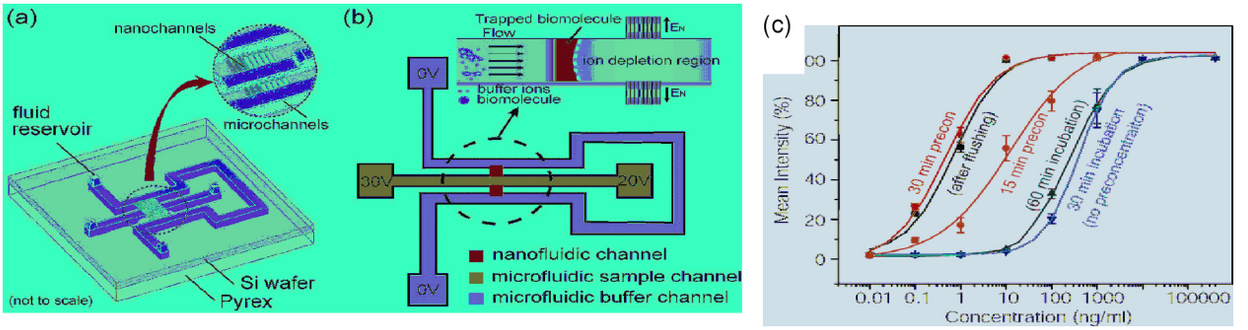

Figure 6. Preconcentration-enhanced immunoassay. a. Schematics of the nanofluidic preconcentration device. The middle sample channel is connected to the U-shaped buffer channel by a nanochannel array with a depth of 40 nm. b. Voltage scheme used for the biomolecule preconcentration and the electrokinetic trapping mechanism. c. Plots showing the dose response of the immunoassay without preconcentration, and with 15-min or 30-min preconcentration. Through maintaining a 30-min on-site preconcentration, this approach can lower the sensitivity limit by about 500-fold from 50 pM to sub 100 fM range (with 10 μgof green fluorescent protein per mL as simulated molecular background molecular background).

1. Wang, Y.-C., and J. Han. 2008. Pre-binding dynamic range and sensitivity enhancement for immuno-sensors using nanofluidic preconcentrator. Lab on a Chip *8: 392–394.*

2. Lee, J. H., Y. A. Song, S. R. Tannenbaum, and J. Han. 2008. Increase of reaction rate and sensitivity of low-abundance enzyme assay using micro/nanofluidic preconcentration chip. Analytical Chemistry *80(9): 3198–3204.*

Performance Enhancements in Strained Nanowire MOSFETs: P. Hashemi, L. Gomez, and J. L. Hoyt

Multigate and "gate-all-around" metal-oxide-semiconductor field effect transistors (MOSFETs) are attractive for deeply scaled CMOS as their geometry improves the ability of the gate to turn the transistor on and off, for very short gate lengths. This enhanced electrostatic control also enables lower channel doping, reducing random dopant fluctuations, which are a significant source of variation for scaled CMOS. Performance boosters such as the use of strain and alternate channel materials to improve carrier transport and maximize the on-current of such devices are essential. The Hoyt group has fabricated the first uniaxial tensile-strained Si nanowire gate-all-around n-MOSFETs. Uniaxial tensile strain is obtained by lateral relaxation of biaxially strained Si on an insulator, by patterning the film into nanoscale wires (width ~15 to 50 nm) and releasing the wires from the substrate. The source and drain pads remained anchored to the substrate (Figure 7). Roughly two times performance enhancement is observed for long-channel strained-Si n-MOSFETs relative to unstrained Si devices, indicating the promise of this technology.

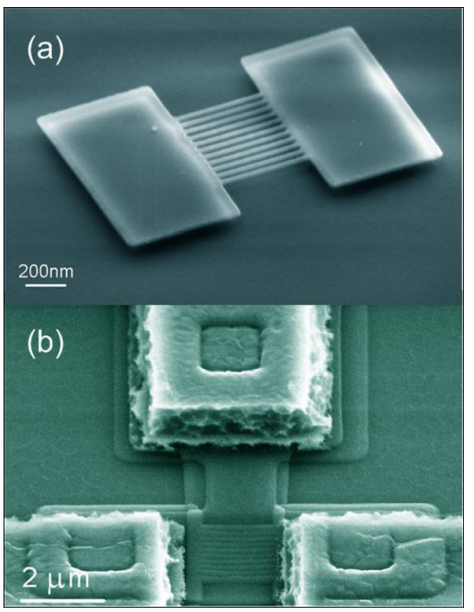

Figure 7. Scanning electron micrograph images of a. 25-nm-wide suspended strained-Si nanowires with source and drain pads attached to the substrate, and b. completed gate-all-around n-MOSFET with 10 nanowires in parallel.

Galvanically Isolated MEMS Relays: A. Weber, A. Slocum, and J. Lang

Professors Lang and Slocum, with graduate student Alexis Weber, are developing galvanically isolated MEMS relays capable of hot-switching electric power at voltages up to several hundred volts and 1 ampere (Figure 8). The applications for these relays range from power handling in equipment to power handling in residential settings. One such relay is shown in Figure 8. It is a cross-bar relay having electrical contacts formed from parallel <111> planes in silicon.

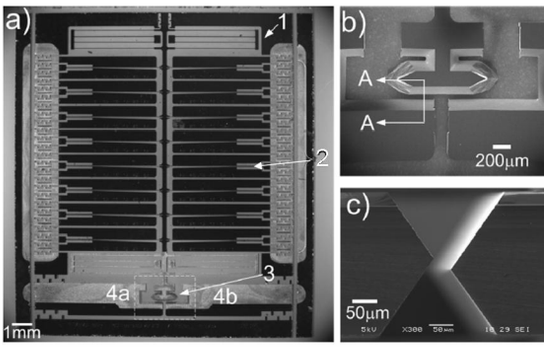

Figure 8. MEMS relay photographs. a. Top view showing: 1. the aft tethers, 2. the zipper actuators, 3. the contacts, and 4. the external contact pads. b. Top view that enlarges the contact region from a. c. Side view of the contacts along the A-A cut in b.

The cross bar is supported by flexible tethers driven by electrostatic zipper actuators. Recently, the relays have been measured to stand off more than 400 V when open and hot switch currents approaching 1 A in the presence of both resistive and inductive loads. The relays exhibit sub-ohm contact resistance and have been run for more than 10^5 cycles without sign of mechanical fatigue.

Large Area, Few-Layer Graphene Films on Arbitrary Substrates by Chemical Vapor Deposition: J. Kong

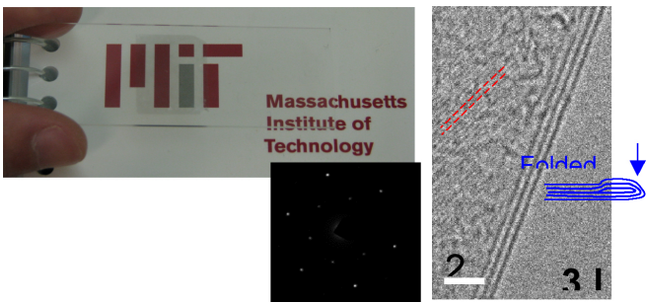

Figure 9. 2-cm x 2-cm graphene film on a glass slide (left). TEM image of a three-layer graphene film (right). Parallel lines on a folded edge reveal the number of graphene layers in the film, as illustrated by the blue diagram. Lattice fringes can be also seen (red dashed lines). Diffraction pattern is also shown (middle bottom). These indicate the high structural quality of the graphene film.

Graphene is the hexagonal arrangement of carbon atoms forming a one-atom-thick planar sheet. The successful isolation of graphene by the microcleaving of highly oriented pyrolytic graphite has opened up exciting possibilities for experimental investigations. Significant attention has been captured by its outstanding properties (such as high mobility (up to 100,000 cm^2/V sec) for both electrons and holes, large current carrying capability (current density > 10^8 A/cm^2), and high mechanical robustness), which render it another materials option for electronic applications. As a result, developing reliable methods to fabricate graphene layers and integrating them with a wide variety of substrates become critical elements in graphene research and large-scale applications. We recently developed a low-cost and scalable technique, via ambient pressure chemical vapor deposition on Ni film, to fabricate large area (~cm^2) films of single- to few-layer graphene and to transfer the films to any type of substrates (Figure 9). These films consist of regions of 1 to ~10 graphene layers. Single- or bilayer regions can be up to 20 μm in lateral size. The films are continuous over the entire area and can be patterned by prepatterning of the Ni structures. The transparency, conductivity, and ambipolar transfer characteristics of the films suggest their potential as another material candidate for electronic and optoelectronic applications.

On-Wafer Integration of Nitride and Si Electronics: J. Chung and T. Palacios

The modern Si chip incorporates very diverse logic circuits, along with mixed-signal and analog circuitry, integrated in a seamless fashion. There is a growing desire to integrate additional wireless modules, power amplifiers, and complex power supply electronics into digital integrated circuits to meet increasing application demands and performance requirements. However, the performance of these new building blocks is limited by the intrinsic material properties of Si. The maximum voltage allowed in Si electronics in combination with the relatively poor velocity of the electrons in this material make the fabrication of ultra-high-speed devices, power electronics, and high-efficiency amplifiers very challenging.

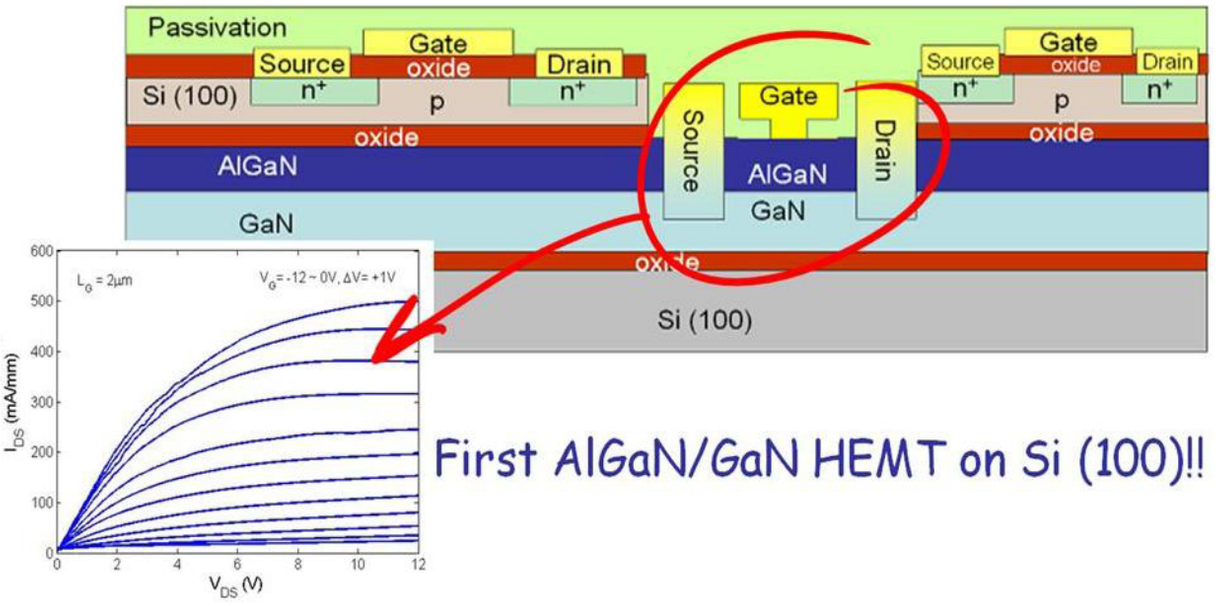

Figure 10. Schematic cross section of the envisioned on-wafer integration of GaN and Si transistors. Our group has recently demonstrated the first integration of GaN transistors on Si (100) substrates. Inset shows the characteristics of one of these first devices.

Nitrides are a new semiconductor family with excellent properties for high-voltage and high-speed electronics. The integration of nitride transistors with Si MOSFETs at the individual transistor level would allow the combination of the outstanding high-frequency and high-power performance of nitride semiconductors with the flexibility and unmatched scaling capability of Si technology. Our group aims to demonstrate the first on-wafer integration of these two devices. Several basic circuit building blocks are also being developed to show the feasibility of this heterogeneous integration, which will revolutionize power electronics, mixed-signal circuits, and wireless communications (Figure 10).

mm-Wave Imaging Using Silicon Integrated Circuits: J. Powell, K. Nguyen, K. Lu, H. Kim (Lincoln Laboratory), and C. G. Sodini

The use of millimeter wavelength (MMW) radiation in imaging systems is well suited for applications such as automotive collision avoidance and concealed weapons detection. By superimposing the signals recorded at antennas configured in an array, the imaging receiver can be focused on a portion of the scene corresponding to a particular pixel. This process, called beamforming, uses constructive interference at the carrier frequency and allows the receiver to be "electronically steered" without any moving mechanical parts. However, very-low-phase noise is required for fine resolution at long range.

Traditionally, beamformers at such high frequencies are built using custom analog technology to ensure precise phase control. Our system performs digital beamforming, allowing for practical and cheap large-scale production and low power consumption. We are designing components with low-phase noise and addressing any excess phase noise by oversampling, averaging, and employing feedback.

The goal of this research is to justify digital beamforming system architecture and establish proof of concept by implementing the most challenging circuit blocks in a silicon-based technology. These blocks include a low-power and low-noise MMW receiver front-end with integrated antenna, a low-phase noise phase-locked loop that can generate the MMW local oscillator frequency, and a delay-locked loop used in a phase-tightening feedback loop to reduce phase noise (Figure 11).

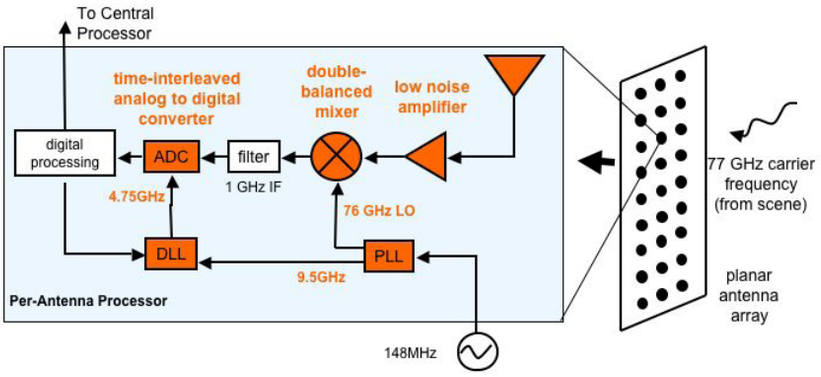

Figure 11. Functional block diagram indicating the key components in the active imaging system.

Integrated Silicon-Photonic Interconnects for Manycore Processors: V. Stojanovic in collaboration with R. Ram, F. Kaertner, J. Hoyt, and H. Smith

We have developed a polysilicon-based photonic device physical design methodology that resulted in the first sub-100-nm photonic test chip in a bulk CMOS process. The measurement results from a 65-nm test chip produced in the Texas Instruments foundry (Figure 12) indicate that optical properties of the polysilicon platform are sufficient to support energy-efficient, high-throughput electrophotonic interconnects for manycore processor to memory communication. This is a major step forward in placing photonic interconnects and devices inside large digital chips in a high-volume, mainstream foundry process. It enables the design of electrooptical core-to-memory network and photonic link circuits that advance the processor throughput by an order of magnitude with respect to optimized electrical solutions, and it overcomes the performance wall emerging from memory bandwidth bottleneck in manycore processors.

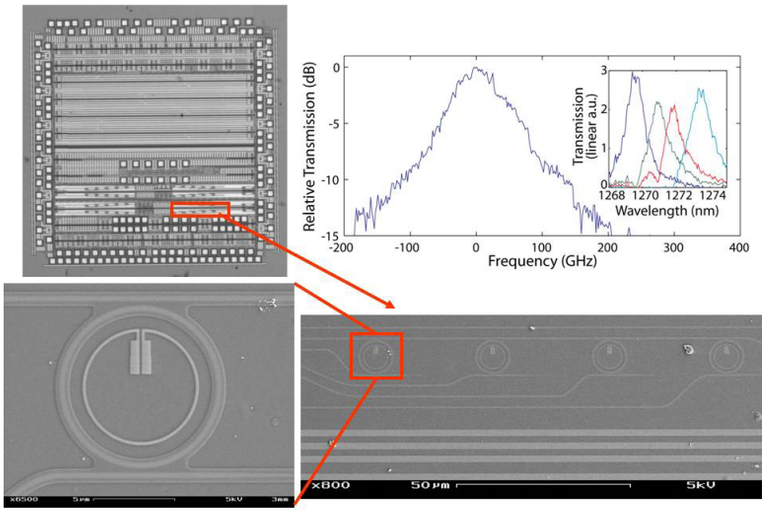

Figure 12. First wavelength division multiplexing filterbank in 65-nm bulk CMOS.

Optofluidic Cell Sorting for Image-Based Cell Isolation: J. Voldman

We have developed a simple, intuitive, low-cost approach for sorting cells following microscopic imaging. This method, which we call OptoFLuCS, uses optical forces to levitate cells out of large arrays of silicone wells (Figure 13). The method is adapted from the well-known optical tweezers, whereby a high-powered laser is focused through a high-numerical aperture objective to confine particles and cells in three dimensions. Instead, we use a low-power (and inexpensive) laser that is sent through a low-numerical aperture (and thus inexpensive) objective. In essence, we create a laser firehose that we use to levitate cells out of wells and into a lateral fluid stream that sweeps them to a collection reservoir. By separating trapping and sorting into two physical domains, we are able to realize a simpler system than would result if we tried to perform all manipulations in each individual domain. In this fashion, we demonstrated image-based cell sorting of cells based on nuclear localization of fluorescence in 10,000 site arrays, along with >150x enrichment of targeted cell populations in an instrument that costs ~$5,000 and that is easily adaptable to many microscopes. This work was reported in a cover article in *Analytical Chemistry*.

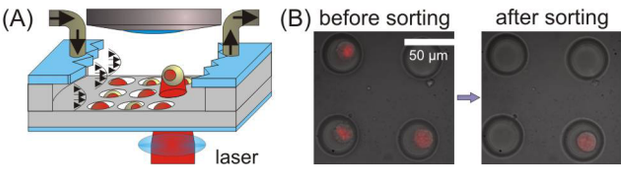

Figure 13. Optofluidic cell sorting. a. Schematic. b. Sorting based on fluorescence localization.

Awards/Honors for Core MTL Faculty

Fellow, Institute of Electrical and Electronics engineers (IEEE)—Akintunde Ibitayo Akinwande, "for contributions to the development of digital self-aligned gate technology and vacuum microelectronic devices"

Fellow, IEEE—Judy Hoyt, "for contributions to silicon-based heterostructure devices and technology"

2008 CAREER award, National Science Foundation—Joel Dawson

Young Investigator Award 2007, Defense Advanced Research Projects Agency—Tomás Palacios

2007 ISSCC Jack Kilby Outstanding Student Paper Award. "A 2.5nJ/b 0.65V 3-to-5GHz Subbanded UWB Receiver in 90nm CMOS" (given at ISSCC 2008)—Anantha P. Chandrakasan (with Fred S. Lee)

2008 DAC/ISSCC Student Design Contest Award, "The Design of a Low Power Carbon Nanotube Chemical Sensor System"—Taeg Sang Cho, K.-J. Lee, Jing Kong, Anantha P. Chandrakasan

IEEE Electron Device Society 2007 Masters Student Award (advisor: Tomás Palacios)—Xu Zhao

IEEE Power Electronics Society Transactions Prize Paper Award, June 2008, (awarded June 2008 for the paper "Resistance Compression Networks for Radio-Frequency Power Conversion")—David Perreault

IEEE Power Electronics Society PESC Conference Prize Paper Award, June 2008 (awarded June 2008 for the paper "A Very High Frequency DC-DC Converter Based on the Class Phi-2 Resonant Inverter")

Affirmative Action

MTL supports the affirmative action goals of the Institute.

Anantha P. Chandrakasan
Director
Professor of Electrical Engineering and Computer Science

More information about the Microsystems Technology Laboratories can be found at http://mtlweb.mit.edu/.