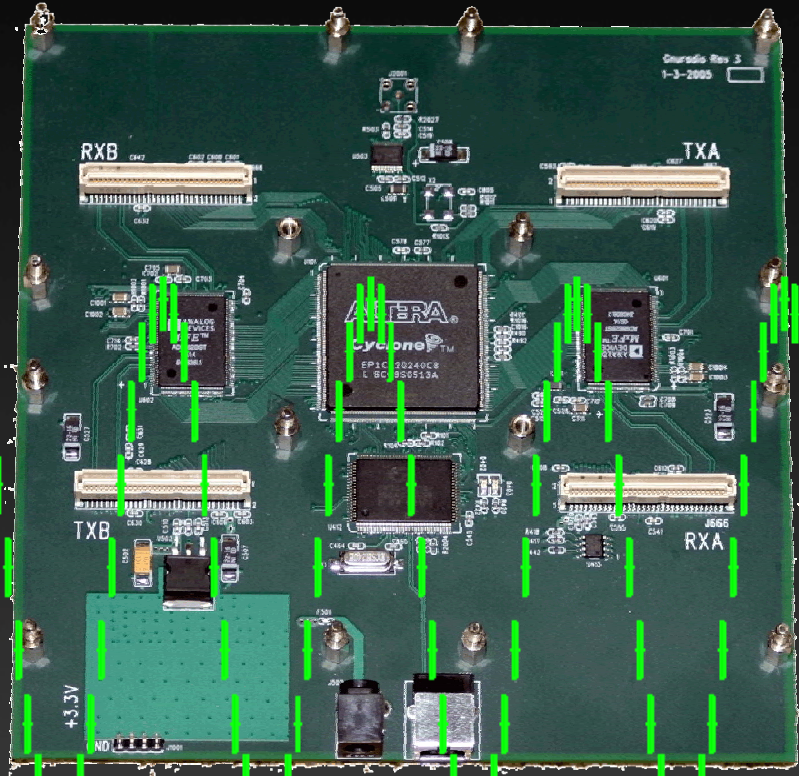


CDMA Control Channel Traffic Analyzer



The Big Picture

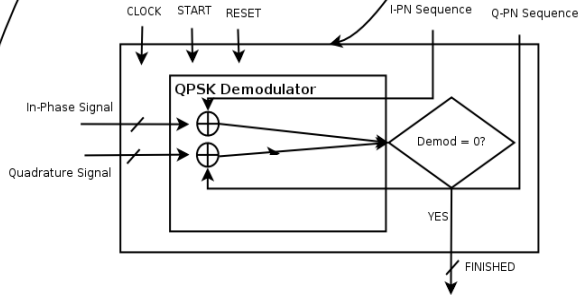
- 1) Tune Radio
- 2) Listen to Pilot Channel
- 3) Listen to Synchronization Channel
- 4) Transmit Sync data via RS232
- 5) Listen to Paging Channel
- 6) Transmit Paging data to PC

Main Control Unit

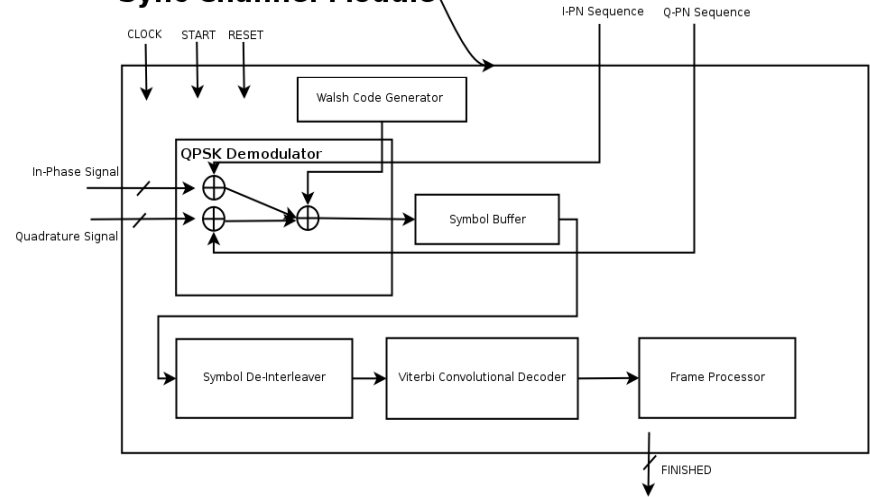
PC Serial Interface

DCM

Pilot Channel Module

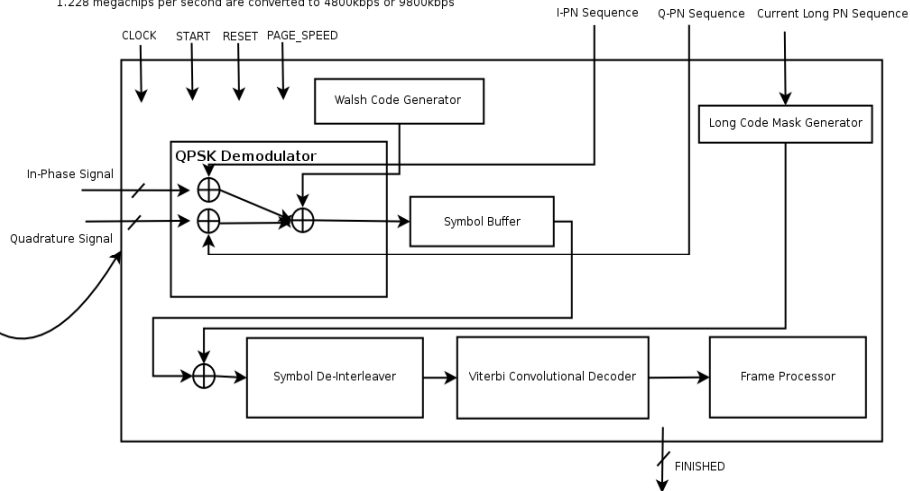


Sync Channel Module



Paging Channel Module

1.228 megachips per second are converted to 4800kbps or 9800kbps



Walsh Lookup Table

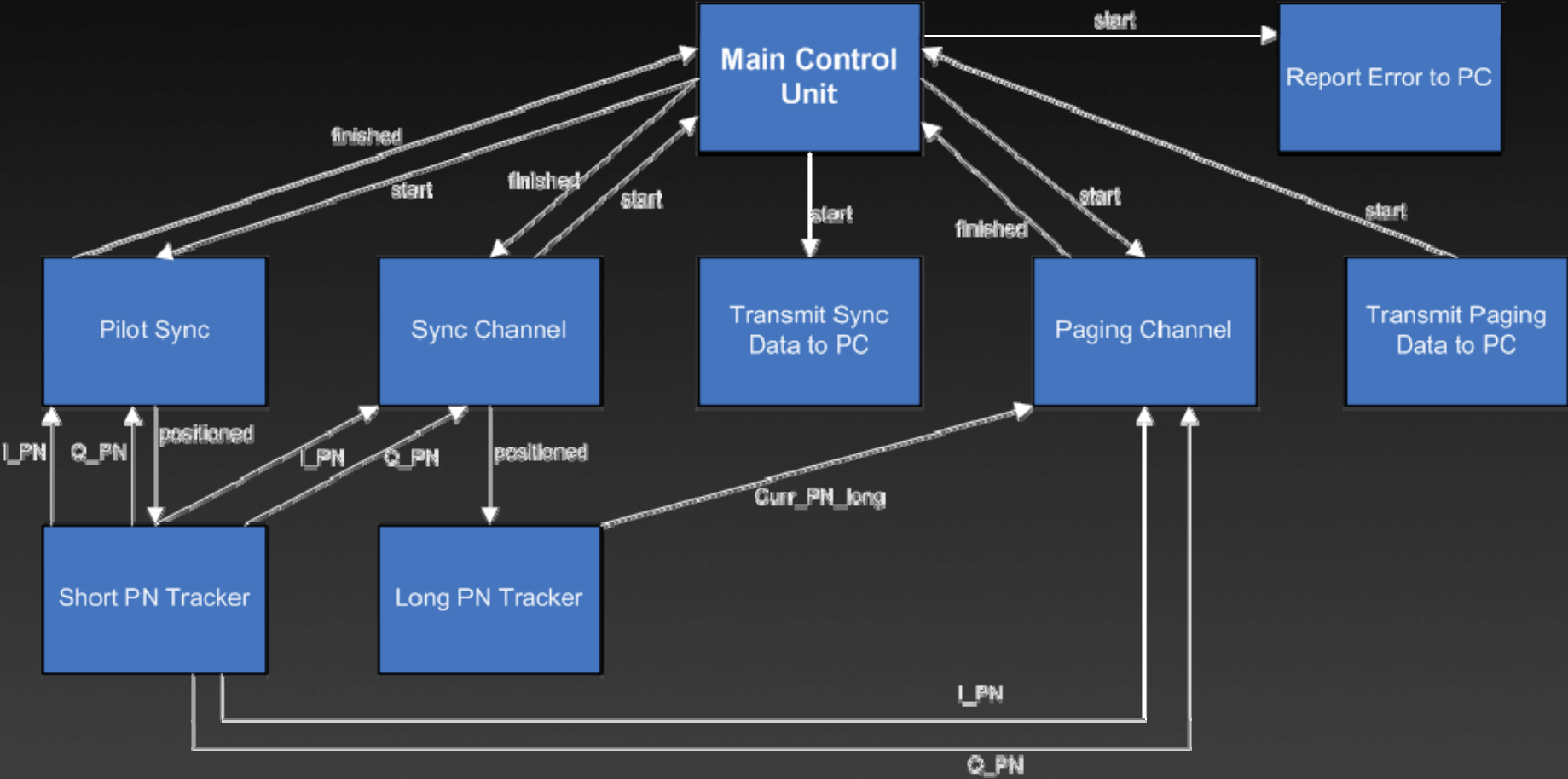
Short PN Sequencer

Long PN Sequencer

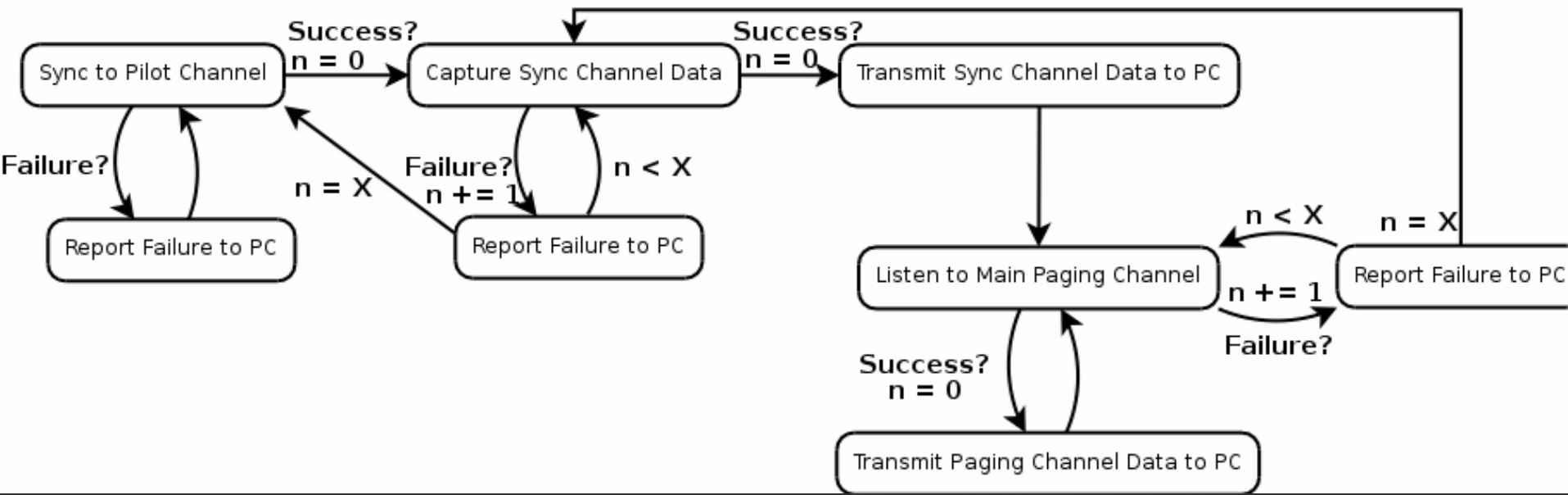
Error Handler

RAM Array Abstraction Module

Main Control Unit



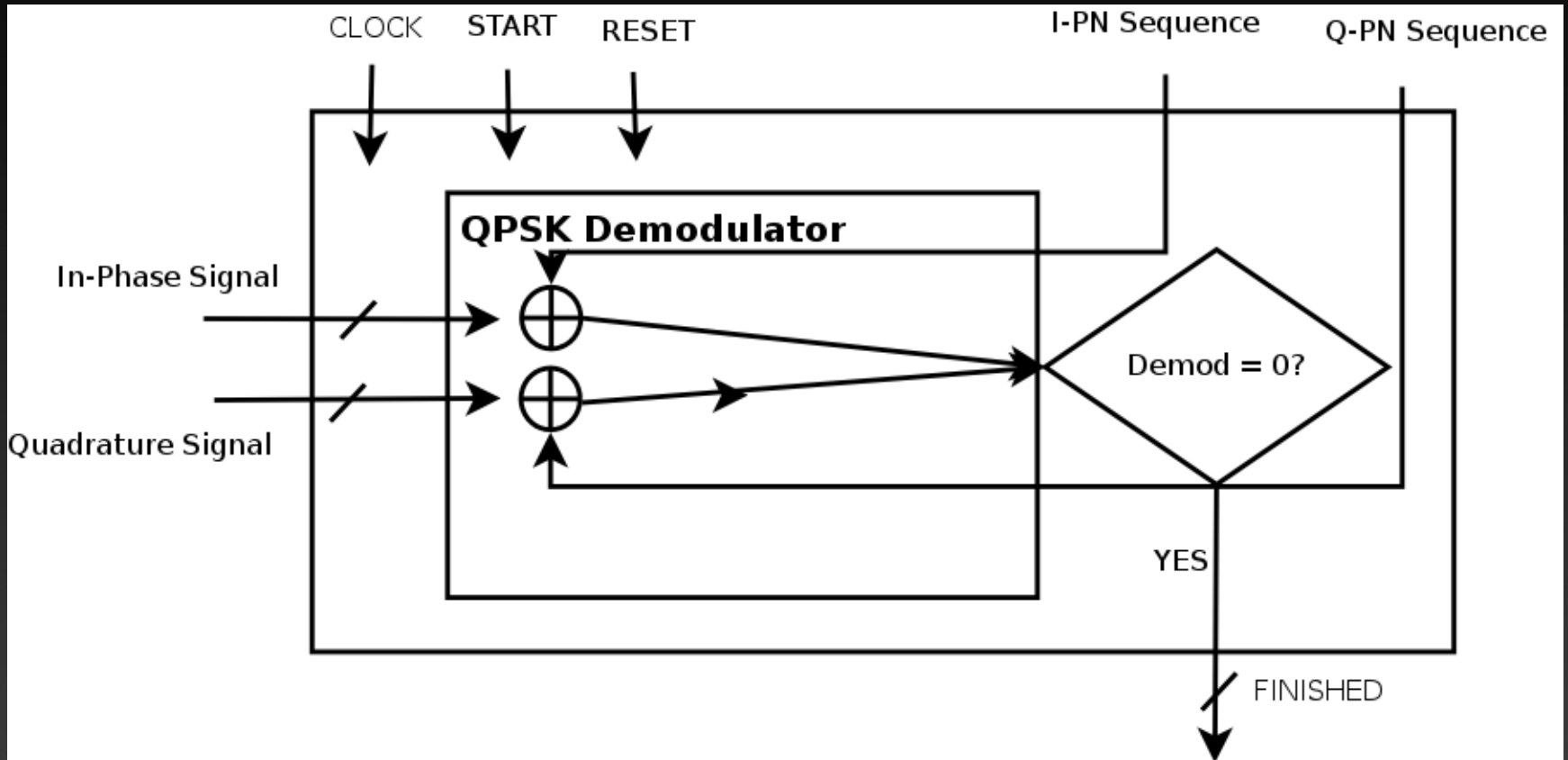
X: Max retries before retrying previous stage



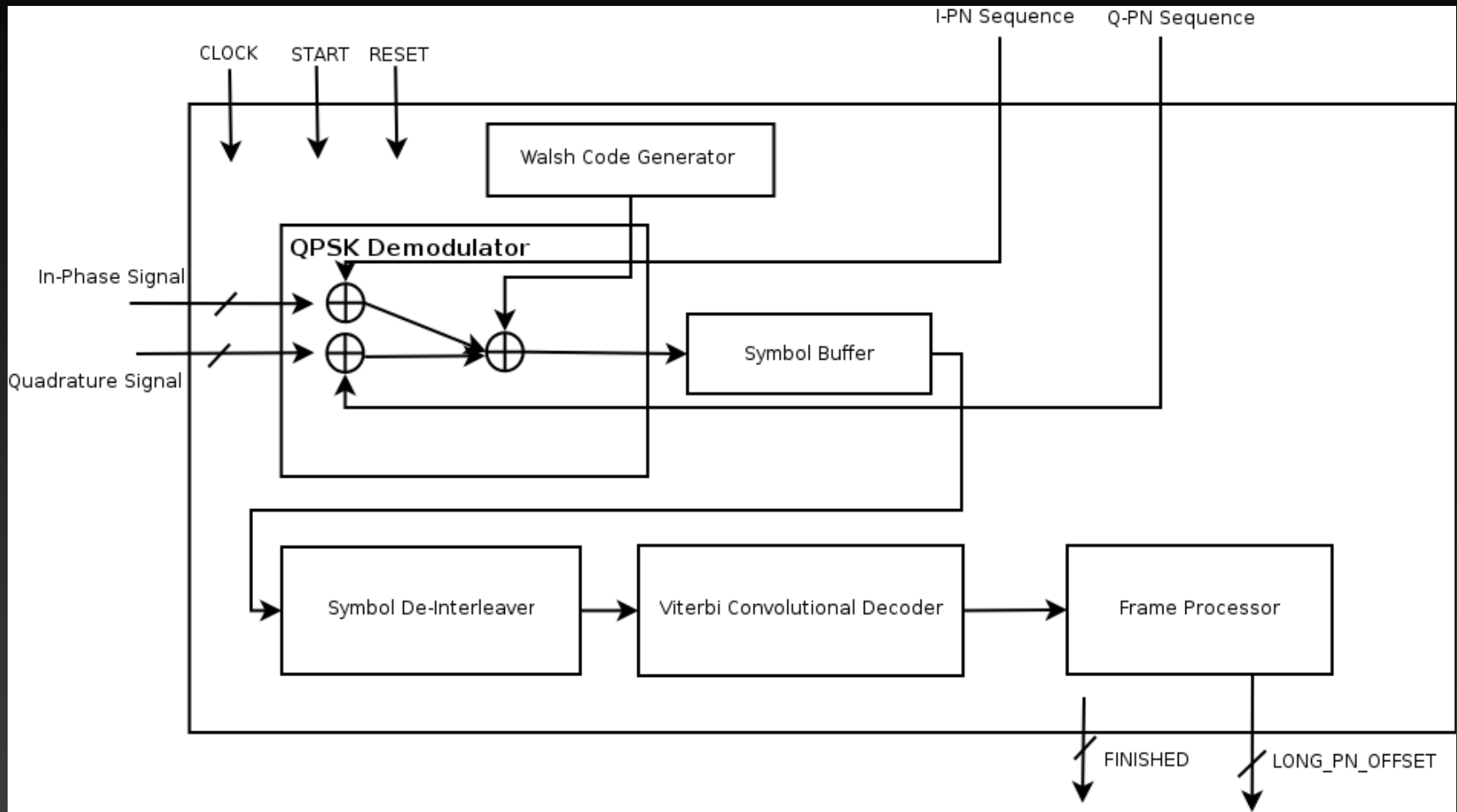
Computer Interface

- High Speed USB->UART converter chip for communications between the FPGA and PC
- Each control unit will have access to talk to host PC
- Software written in Python will interface with the USRP to set center frequency
- USRP transmits I/Q data to PC, which then forwards it to the FPGA

Pilot Channel

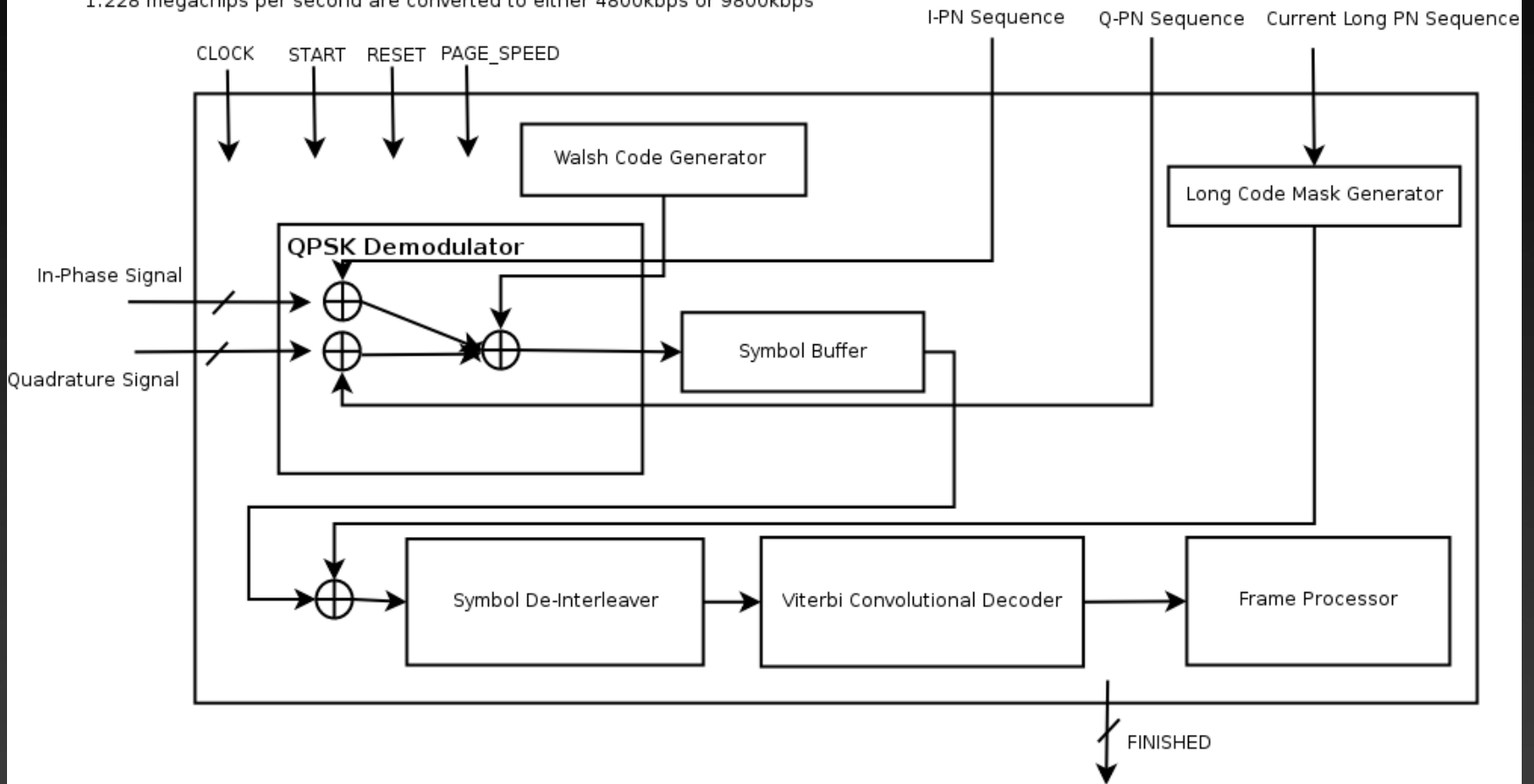


Synchronization Channel



Paging Channel

1.228 megachips per second are converted to either 4800kbps or 9800kbps



and perhaps in the future...
Full-duplex voice conversations