

Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science
6.111 – Introductory Digital Systems Laboratory (Spring 2007)

Final Project Check Off Sheet: CDMA Control Channel Traffic Analyzer

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Must show the TA at the beginning of check off:

- Overall block diagram
- State transition diagram for the Main FSM
- State transition diagram for the Pilot Channel FSM
- State transition diagram for the Sync Channel FSM

Be able to demonstrate functioning components:

- USRP tunes to correct frequency and streams to FPGA (*RJ*)
- Verify two-way serial communication link (*Zack*)
- Be able to generate Walsh Codes (*Zack*)
- Generate I & Q PN Sequences accurately (*RJ*)
- Generate Long PN Sequence accurately (*RJ*)
- Ensure proper state transitions in FSMs (*RJ*)
- Demonstrate proper QPSK demodulation (*Zack*)
- Demonstrate proper de-interleaving (*Zack*)
- Interpret, parse and display transmitted data to the computer screen (*Zack*)
- Demonstrate functioning Viterbi de-encoding (*RJ*)

Be able to demonstrate a working project:

- Synchronize with Pilot Channel (LED displays show zeros, indicating properly demodulated Pilot Channel data)
- Display Sync Channel data on PC