Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science
6.111 Introductory Digital Systems Laboratory (Spring 2007)

Final Project Check Off Sheet

Project Title: Wireless Headphones

Student Names: Nivedita Chandrasekaran, Jessica Nesvold, Aditi Shrikumar

TA Name: David Wentzloff

TA Signature/Date:

System Level

- ☐ Transmit a 3 minute audio file wirelessly to the receiving headphone set.
- ☐ Compresses the digital signal into a packet form compatible with the wireless transmitter and receiver.
- ☐ Transmits and receives packets from distances of at least 20 feet.
- ☐ Decompresses the received packets.
- ☐ Converts the decompressed digital packets back into analog.
- ☐ Outputs the analog signal to headphones.

ADC and DAC (Aditi)

- ☐ Finite state machine transition diagrams, block diagrams, and Verilog code.
- ☐ 5x16bit interface between ADC/DAC and compression/decompression modules.
- ☐ Implement serial interface to ADC/DAC.

Compression/Decompression (Jessica)

- ☐ Finite State Machine transition diagrams, block diagrams, and Verilog code.
- ☐ Verilog compression algorithm for use with signed 16-bit integer inputs.
- ☐ Verilog decompression algorithm that takes in compressed packets and outputs signed 16-bit integers.
- ☐ Working buffer for interfacing to wireless module.

Wireless (Nivedita)

- ☐ Finite State Machine transition diagrams, block diagrams, and Verilog code.

- [ ] Major FSM properly transitions between transmission, reception, and configuration states.
- [ ] Wireless chip reset and configured correctly (panID, device ID).
- [ ] Transmits packets from FPGA transmit FIFO buffer, resends if necessary.
- [ ] Receives packets into FPGA reception FIFO buffer, sends ACK if CRC is correct.
- [ ] Transmit a 10 byte packet of data across the lab.