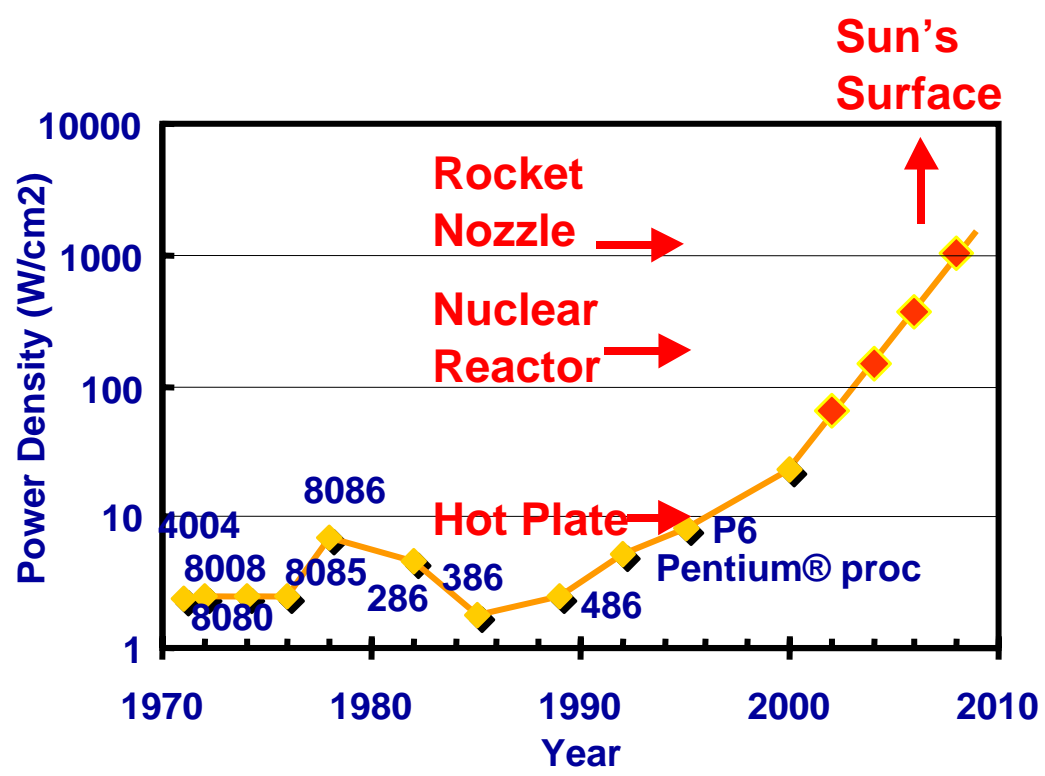# L16: Power Dissipation in Digital Systems

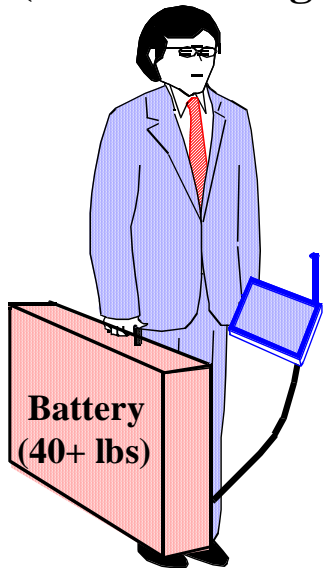# Problem #1: Power Dissipation/Heat
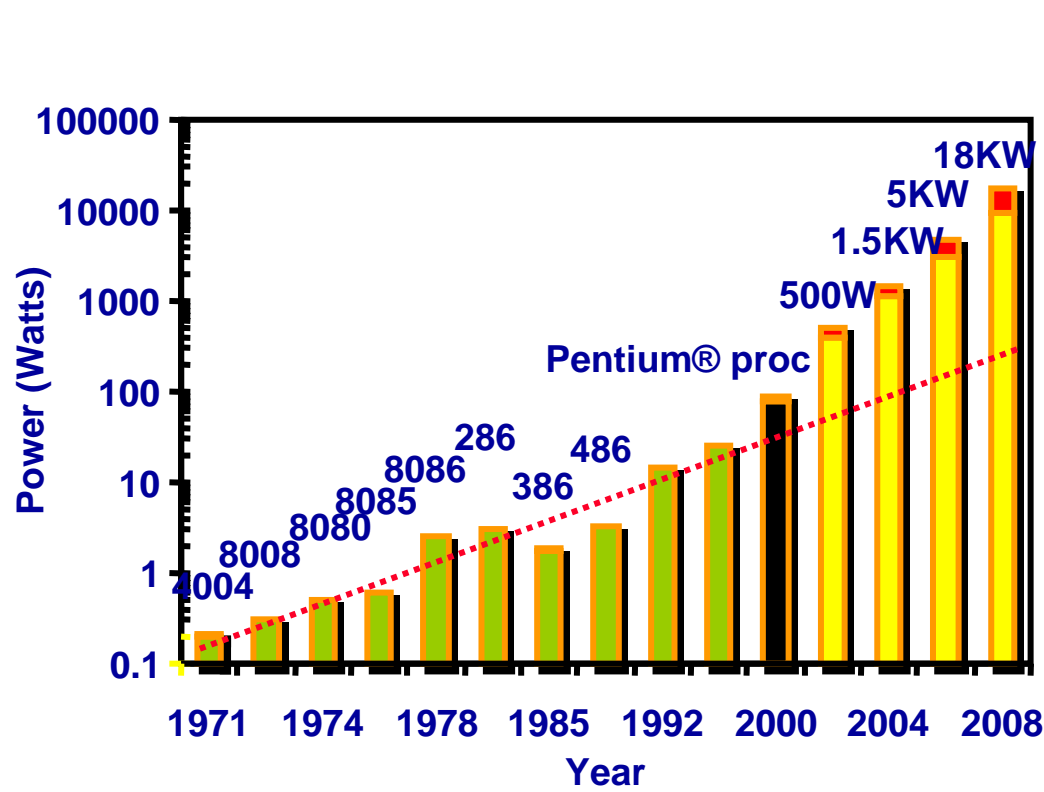
Courtesy Intel (S. Borkar)

How do you cool these chips??

Problem #2: Energy Consumption

Nominal Capacity (Watt-hours / lb) vs. Year chart showing Rechargable Lithium, Ni-Metal Hydride, and Nickel-Cadmium curves.
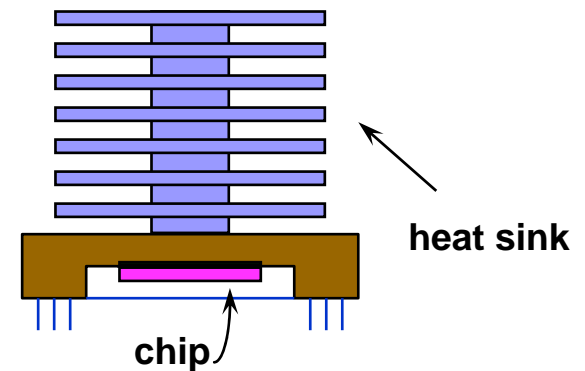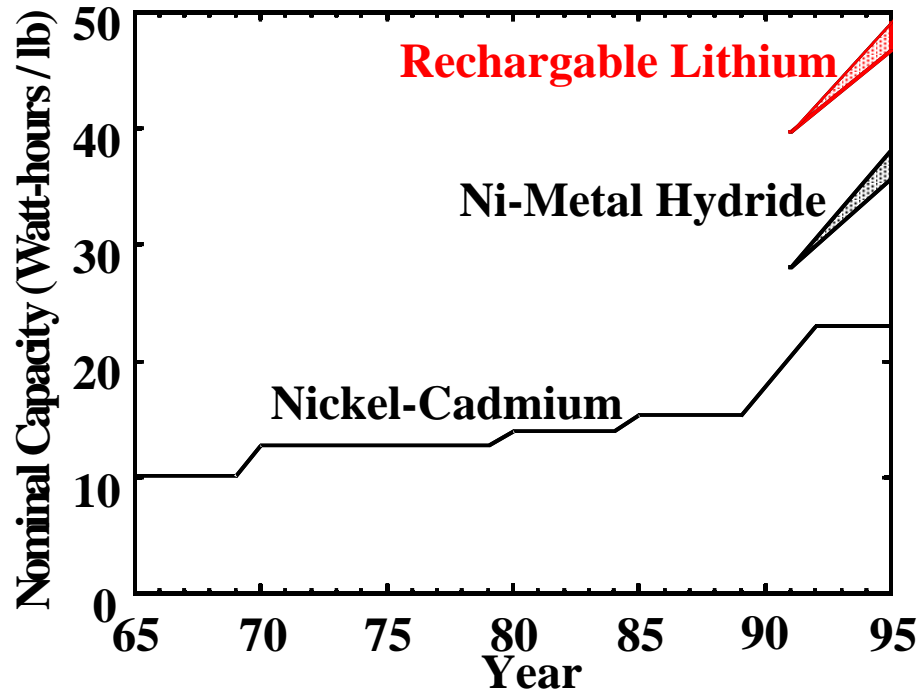
(from Jon Eager, Gates Inc. , S. Watanabe, Sony Inc.)
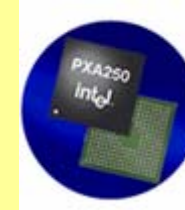
Battery (40+ lbs)

The Energy Problem

7.5 cm³
AA battery

Alkaline:
~10,000J

What can One Joule of energy do?
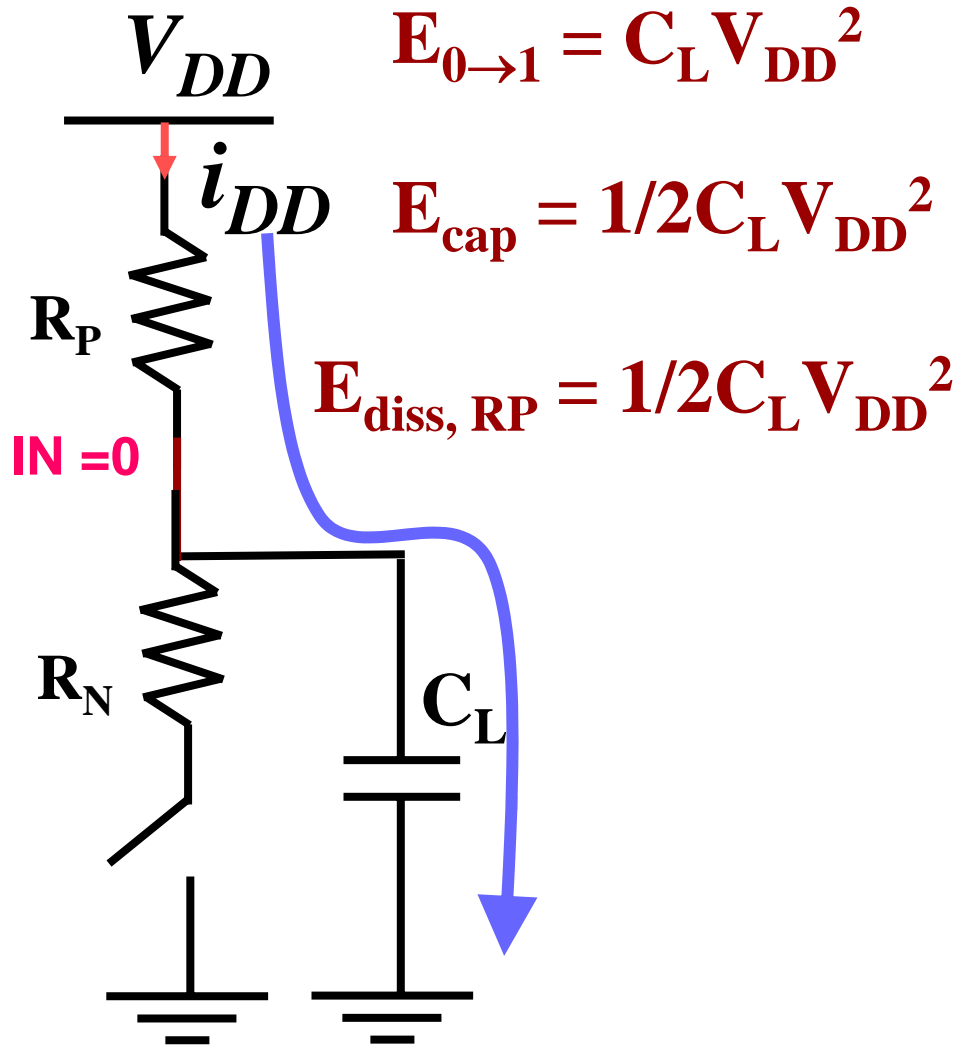
| Mow your lawn for 1 ms | Operate a processor for ~ 7s | Send a 1 Megabyte file over 802.11b |

No Moore's law for batteries…

Today: Understand where power goes and ways to manage it

Dynamic Energy Dissipation

Charging

$$E_{0 \to 1} = C_L V_{DD}^2$$

$$E_{cap} = 1/2 C_L V_{DD}^2$$

$$E_{diss, RP} = 1/2 C_L V_{DD}^2$$

V_{DD}

i_{DD}

R_P

IN =0

R_N

C_L

Discharging

V_{DD}

R_P

$$E_{diss,RN} = 1/2 C_L V_{DD}^2$$

IN =1

R_N

C_L

$$P = C_L V_{DD}^2 f_{clk}$$

The Transition Activity Factor $\alpha_{0 \to 1}$
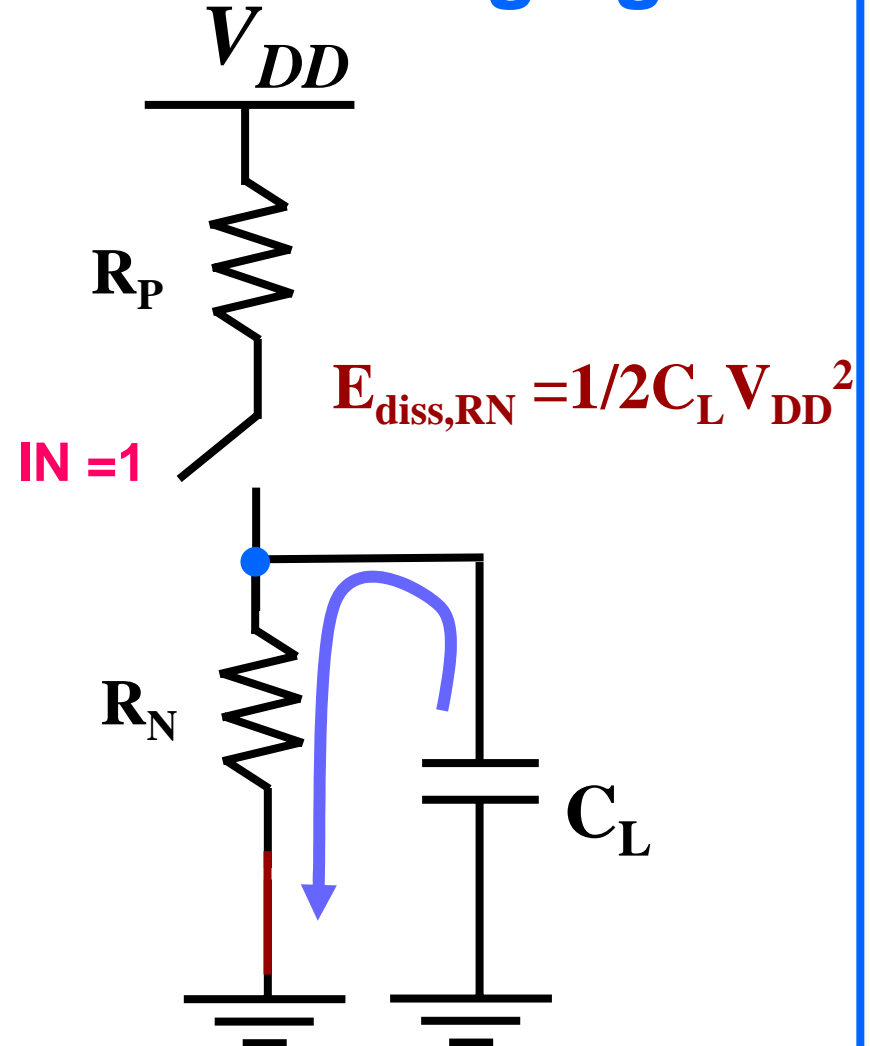
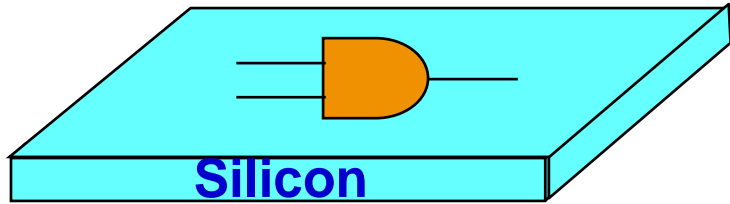| Current Input	Next Input	Output Transition
00	00	1 –> 1
00	01	1 –> 1
00	10	1 –> 1
00	11	1 –> 0
01	00	1 –> 1
01	01	1 –> 1
01	10	1 –> 1
01	11	1 –> 0
10	00	1 –> 1
10	01	1 –> 1
10	10	1 –> 1
10	11	1 –> 0
11	00	0 –> 1
11	01	0 –> 1
11	10	0 –> 1
11	11	0 –> 0

A ——□o— Z
B ——
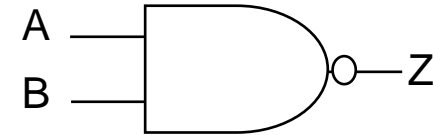
Assume inputs (A,B) arrive at f and are uniformly distributed

What is the average power dissipation?

$$\alpha_{0 \to 1} = 3/16$$

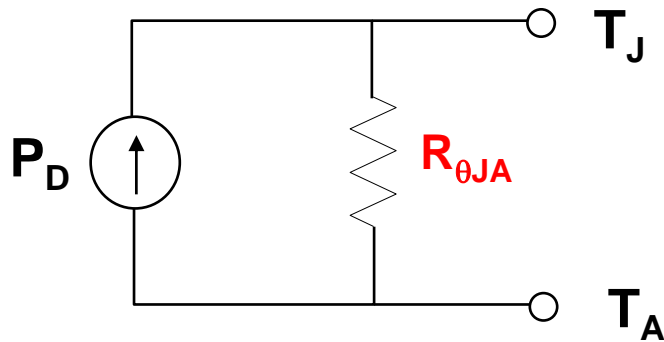$$P = \alpha_{0 \to 1} \, C_L \, V_{DD}^2 \, f$$

Junction (Silicon) Temperature

Simple Scenario

Silicon

$$T_j - T_a = R_{\theta JA} \, P_D$$

$R_{\theta JA}$ **is the thermal resistance between silicon and Ambient**

P_D $R_{\theta JA}$ T_J T_A

$$T_j = T_a + R_{\theta JA} \, P_D$$

Make this as low as possible

Realistic Scenario

Silicon T_J

Case T_C

Sink T_S

T_A

P_D $R_{\theta JC}$ T_J

T_C

$R_{\theta CS}$ T_S

$R_{\theta SA}$ T_A
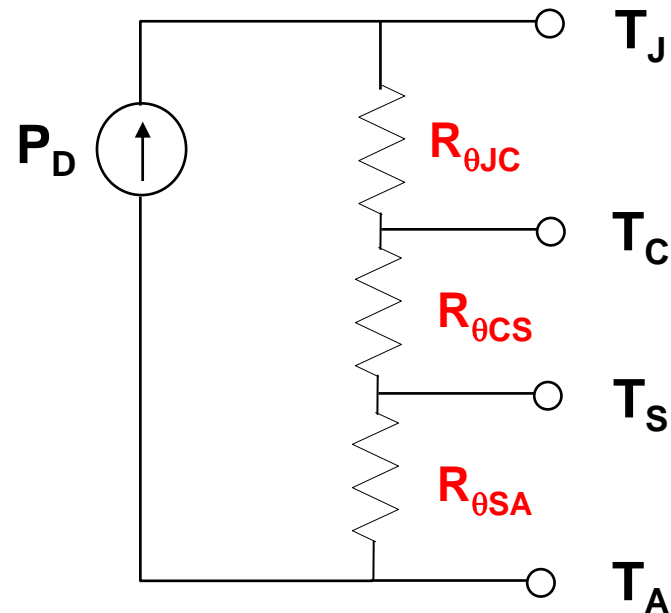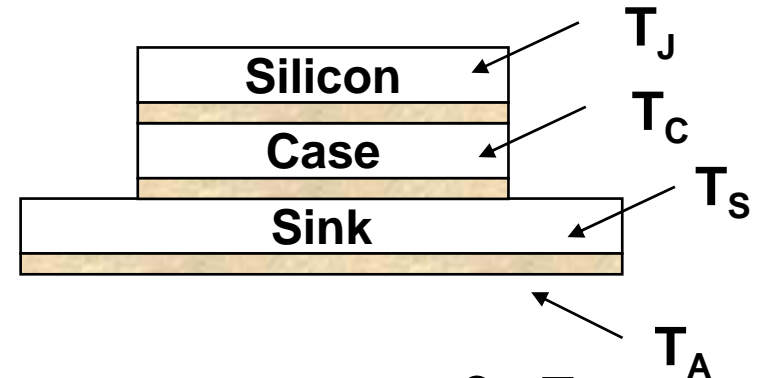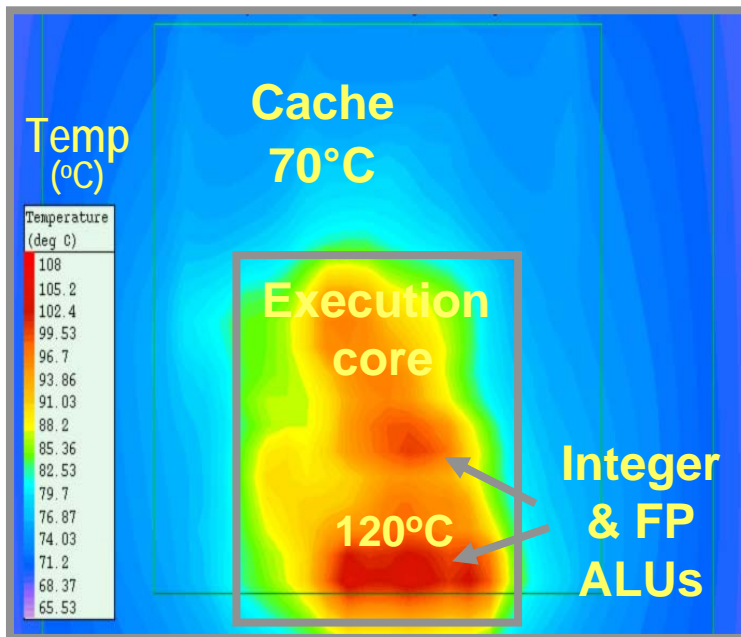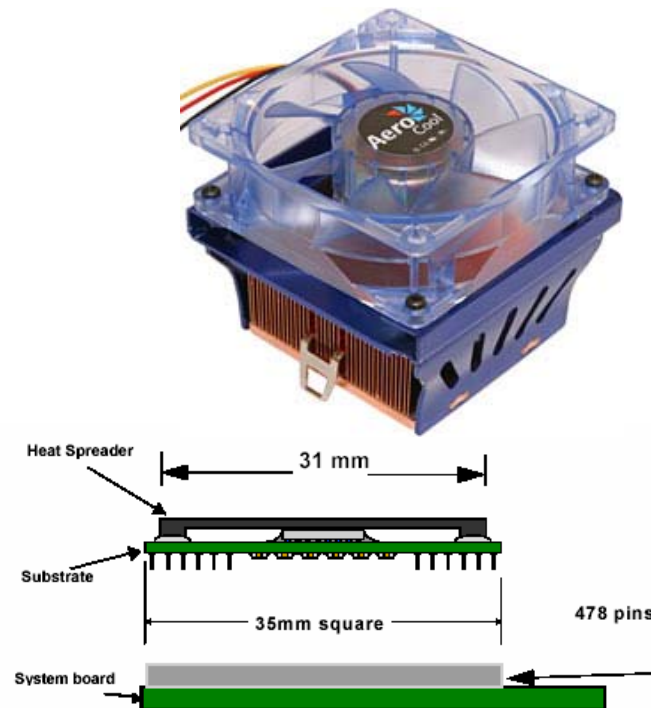
$$R_{\theta CA} = R_{\theta CS} + R_{\theta SA}$$

is minimized by facilitating heat transfer (bolt case to extended metal surface – heat sink)

Intel Pentium 4 Thermal Guidelines

- **Pentium 4 @ 3.06 GHz dissipates 81.8W!**

- **Maximum T_C = 69 °C**

- **R_{CA} < 0.23 °C/W for 50 C ambient**

- **Typical chips dissipate 0.5-1W (cheap packages without forced air cooling)**

Temp (°C)

Temperature (deg C)

108
105.2
102.4
99.53
96.7
93.86
91.03
88.2
85.36
82.53
79.7
76.87
74.03
71.2
68.37
65.53

Cache 70°C

Execution core

120°C

Integer & FP ALUs

Courtesy of Intel (Ram Krishnamurthy)

Heat Spreader

31 mm

Substrate

35mm square

478 pins

System board

Processor and Core Frequency	Thermal Design Power[1,2] (W)
Processors with VID=1.500V	
2 GHz	52.4
2.20 GHz	55.1
2.26 GHz	56.0
2.40 GHz	57.8
2.50 GHz	59.3
2.53 GHz	59.3
Processors with VID=1.525V	
2 GHz	54.3
2.20 GHz	57.1
2.26 GHz	58.0
2.40 GHz	59.8
2.50 GHz	61.0
2.53 GHz	61.5
2.60 GHz	62.6
2.66 GHz	66.1
2.80 GHz	68.4
Processors with multiple VIDs	
2 GHz	54.3
2.20 GHz	57.1
2.26 GHz	58.0
2.40 GHz	59.8
2.50 GHz	61.0
2.53 GHz	61.5
2.60 GHz	62.6
2.66 GHz	66.1
2.80 GHz	68.4
3.06 GHz	81.8

$$P = \alpha_{0->1} \, C_L \, V_{DD}^2 \, f$$

- **Reduce Transition Activity or Switching Events**

- **Reduce Capacitance (e.g., keep wires short)**

- **Reduce Power Supply Voltage**

- **Frequency is typically fixed by the application, though this can be adjusted to control power**

Optimize at all levels of design hierarchy

Clock Gating is a Good Idea!

Clock gating reduces activity and is the most common low-power technique used today

Global Clock

Enable_Adder

Adder Off

Adder Clock

+

Multiplier On

Enable_Multiplier

Multiplier Clock

X
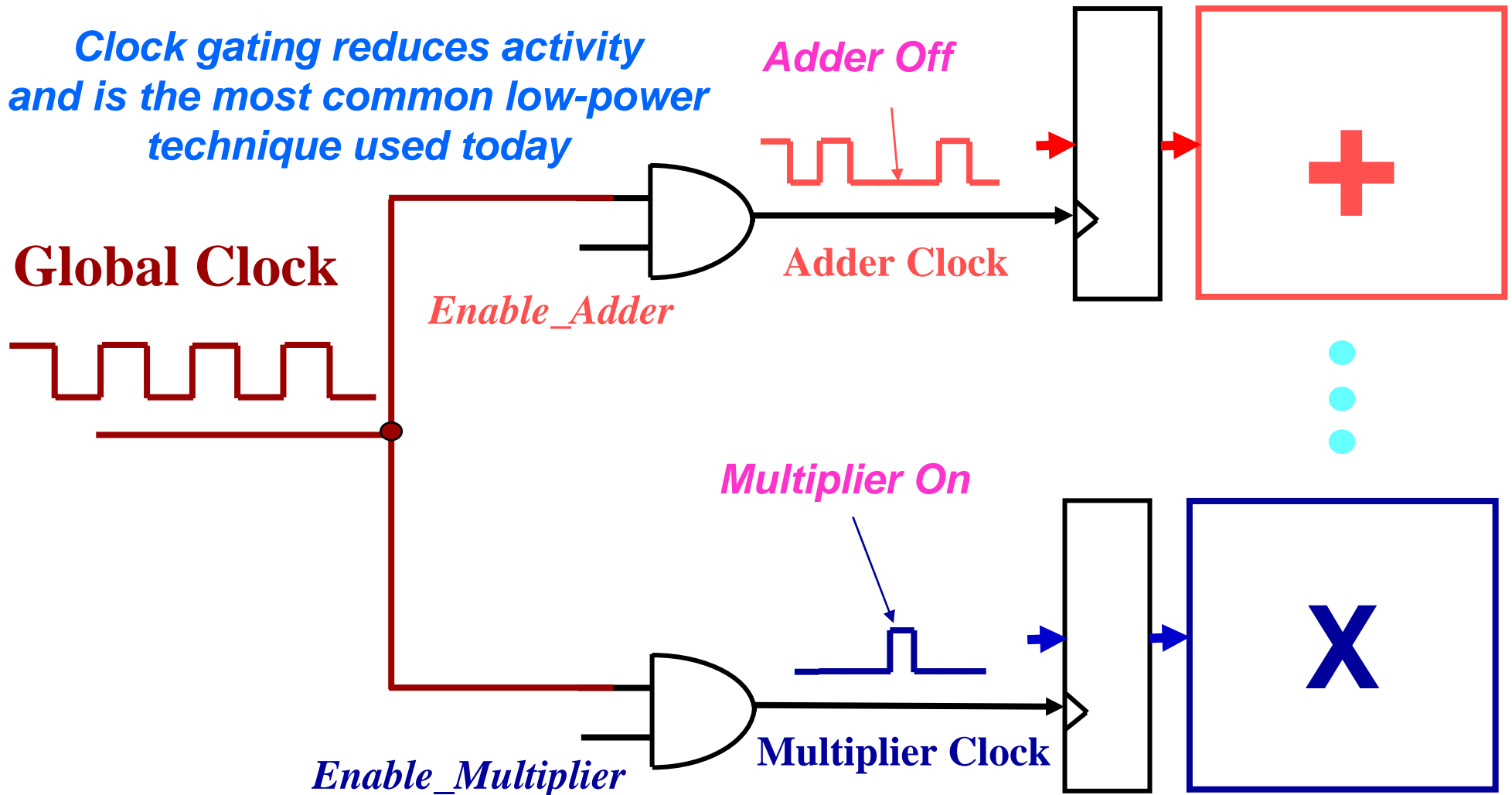
100's of different clocks in a microprocessor

Clock Gating Reduces Energy, does it reduce Power?

Does your GHz Processor run at a GHz?

Processor

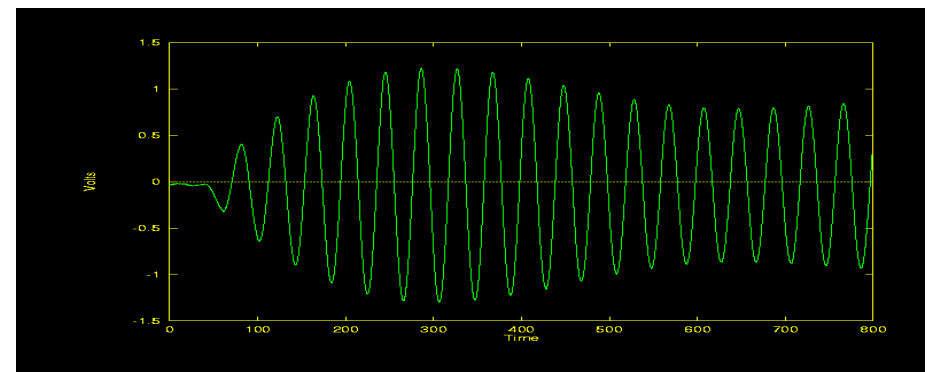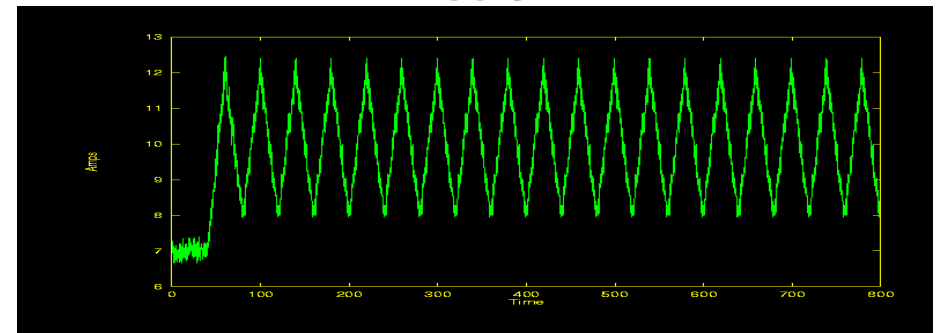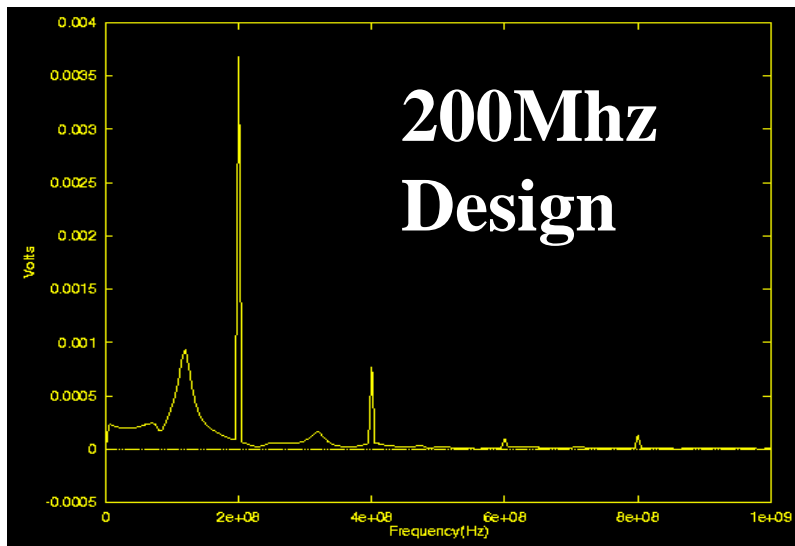**Chip Activity Control**
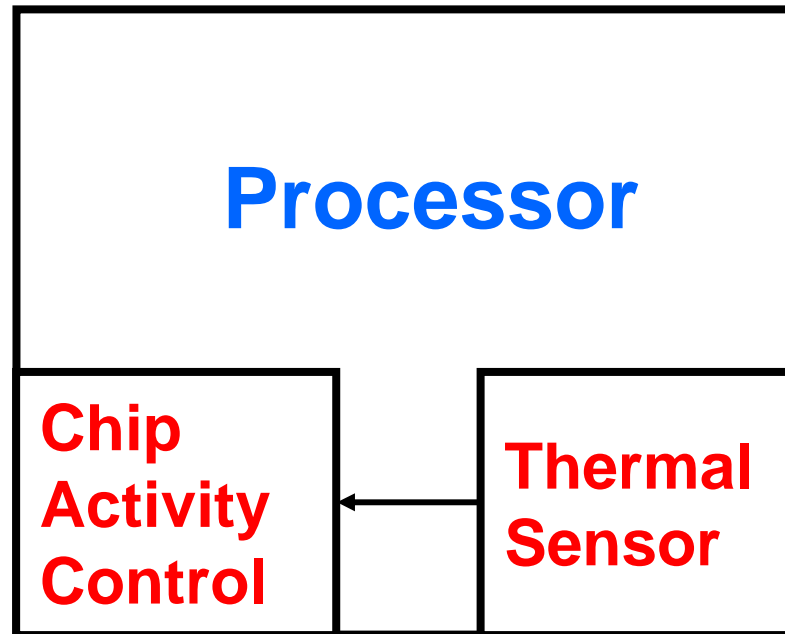
Thermal Sensor

- **Note that there is a difference between average and peak power**
- **On-chip thermal sensor (diode based), measures the silicon temperature**
- **If the silicon junction gets too hot (say 125 °C), then the activity is reduced (e.g., reduce clock rate or use clock gating)**
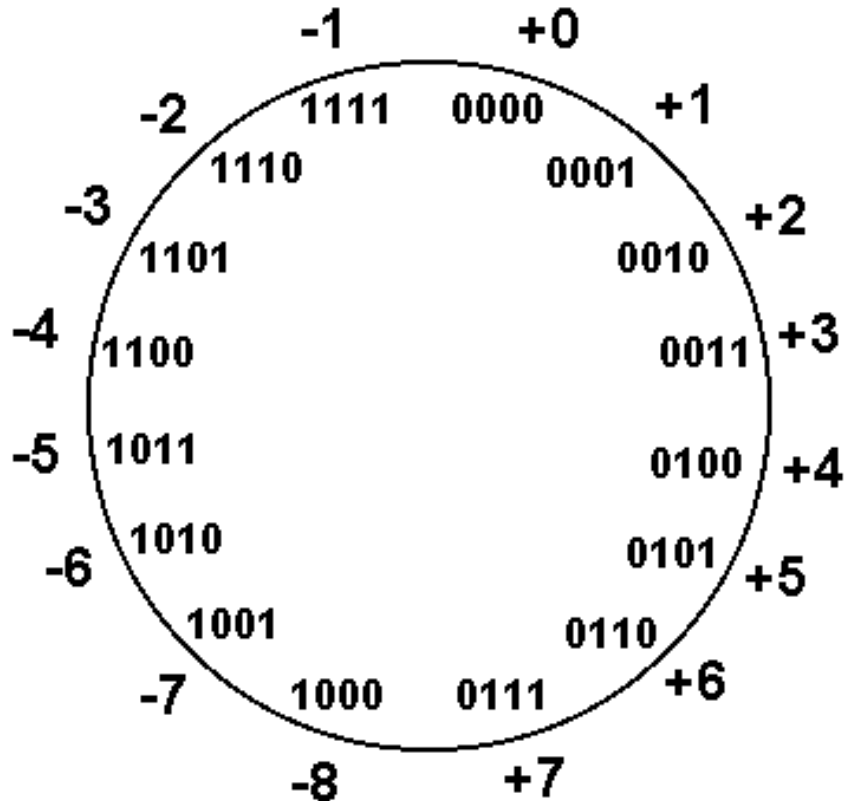
Use of Thermal Feedback

Power Supply Resonance

L_{board} $L_{package}$ R_{grid}
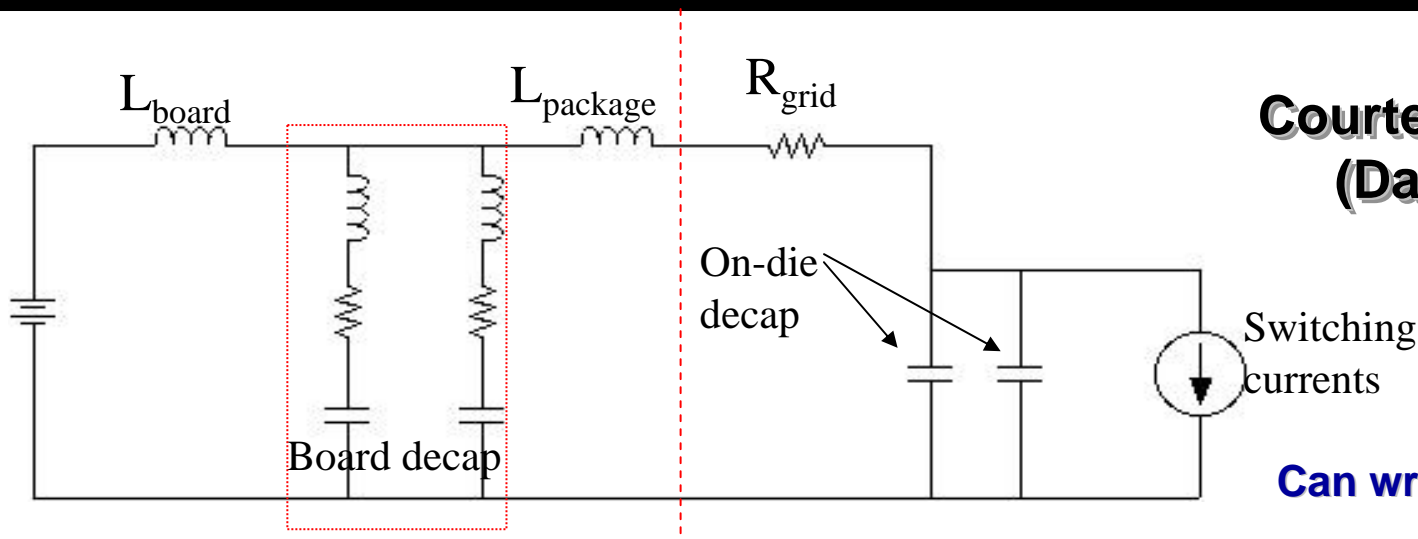
Courtesy of Motorola
(David Blaauw)

On-die decap

Switching currents

Board decap

Can write a Virus to Activate

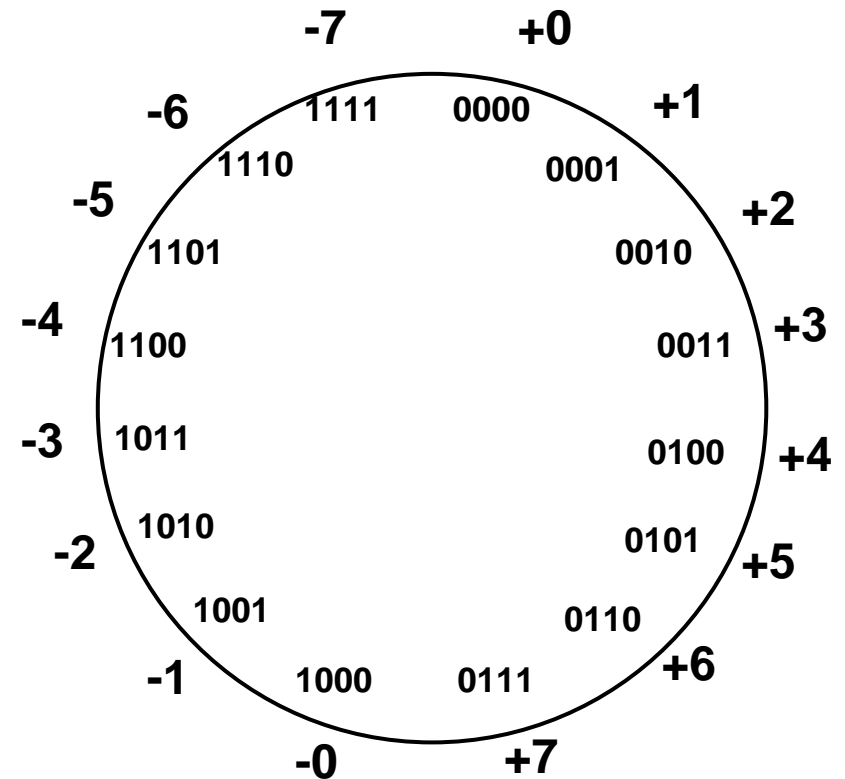**Power Supply Resonance!**

200Mhz Design

Number Representation:
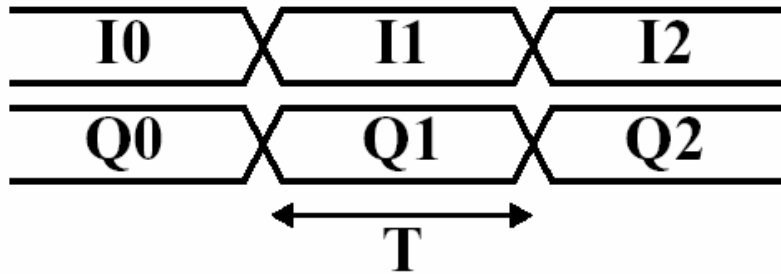# Two's Complement vs. Sign Magnitude
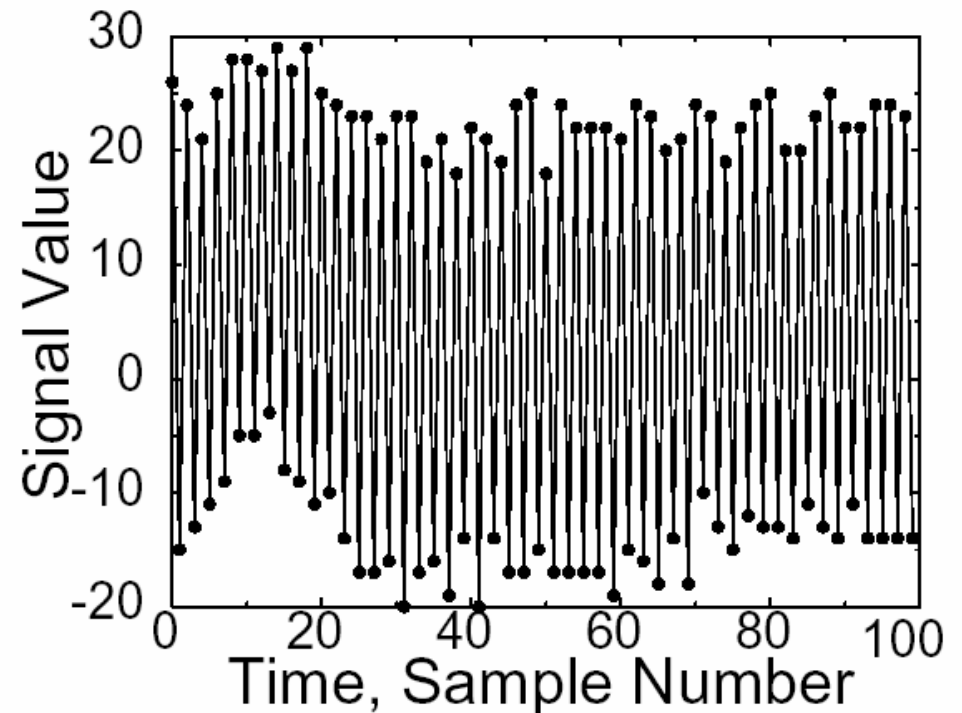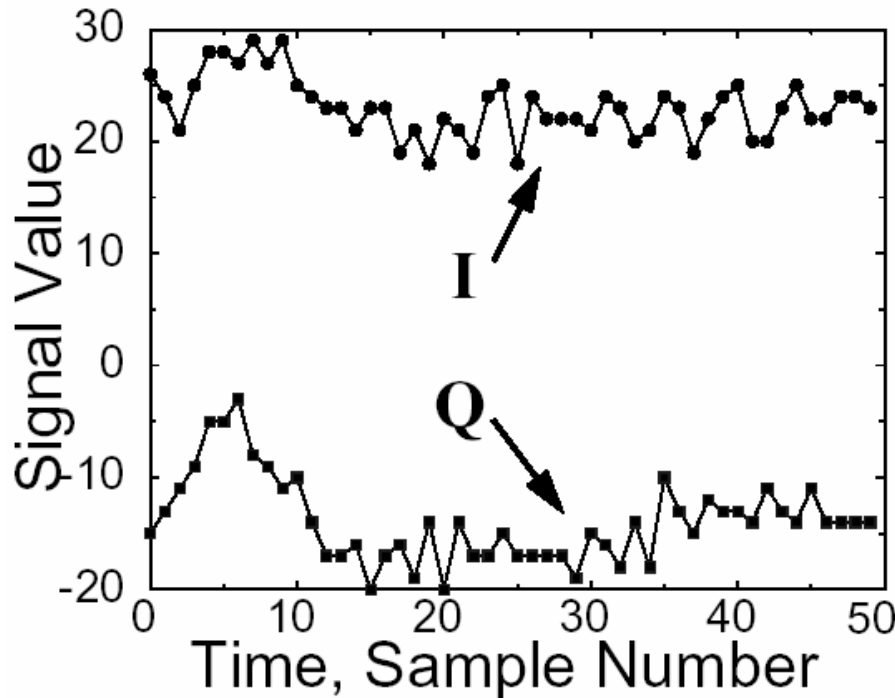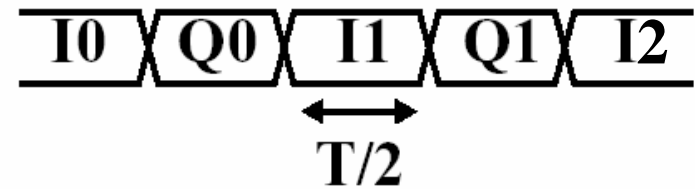
Two's complement

Sign-Magnitude

Consider a 16 bit bus where inputs toggles between +1 and −1 (i.e., a small noise input) Which representation is more energy efficient?

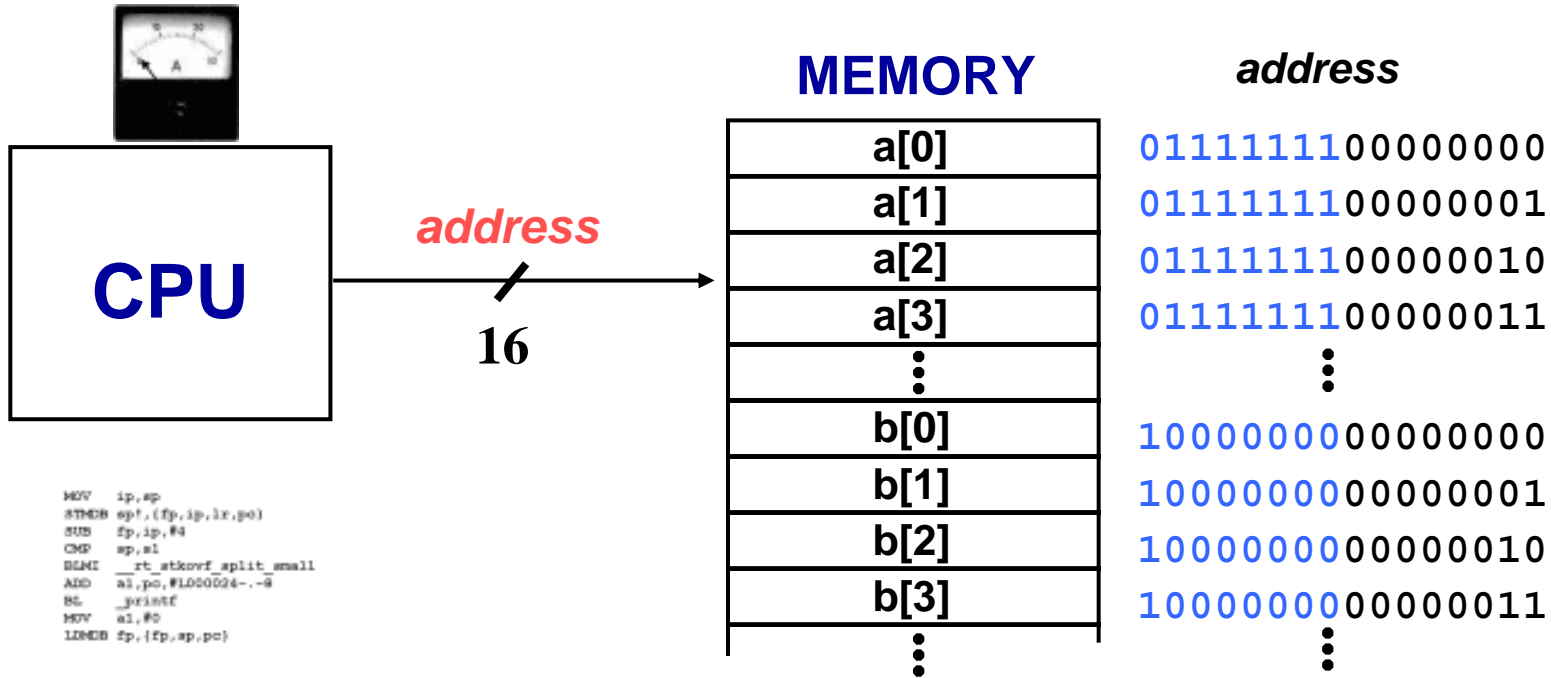# Time Sharing is a Bad Idea

Parallel busses for I,Q

Time-shared bus for I,Q

Time Sharing Increases Switching Activity

Not just a 6-1 Issue: "Cool" Software ???

CPU

address

16

```
MOV    ip,sp
STMDB  sp!,{fp,ip,lr,pc}
SUB    fp,ip,#4
CMP    sp,sl
BLMI   __rt_stkovf_split_small
ADD    al,pc,#L000024-.-8
BL     _printf
MOV    al,#0
LDMDB  fp,{fp,sp,pc}
```

MEMORY   *address*

a[0]	0111111100000000
a[1]	0111111100000001
a[2]	0111111100000010
a[3]	0111111100000011
⋮	⋮
b[0]	1000000000000000
b[1]	1000000000000001
b[2]	1000000000000010
b[3]	1000000000000011

float a [256], b[256];
float pi= 3.14;

for (i = 0; i < 255; i++) {
   a[i] = sin(pi * i /256);
   b[i] = cos(pi * i /256);
}

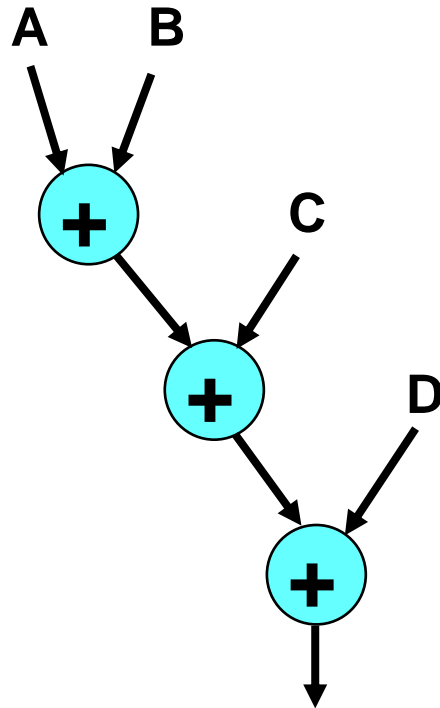512(8)+2+4+8+16+32+64+128+256
= 4607 bit transitions

float a [256], b[256];
float pi= 3.14;

for (i = 0; i < 255; i++) {a[i] = sin(pi * i /256);}
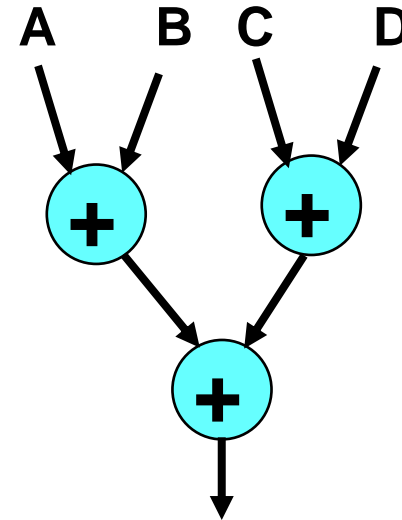**for (i = 0; i < 255; i++) {b[i] = cos(pi * i /256);}**

2(8)+2(2+4+8+16+32+64+128+256)
= 1030 transitions

Glitching Transitions

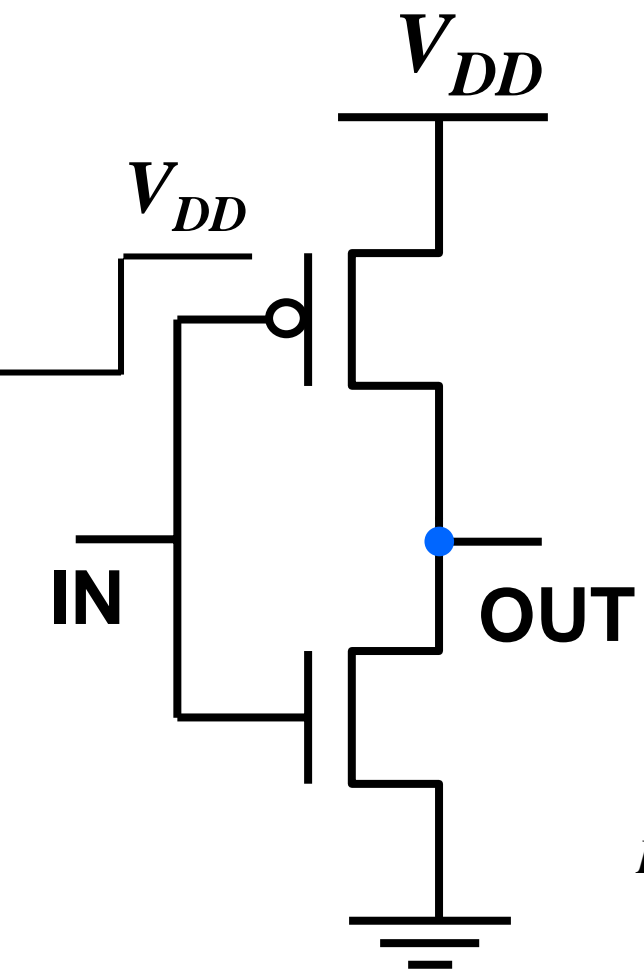## Chain Topology

A B

C

D

$$(((A+B) + C)+D)$$

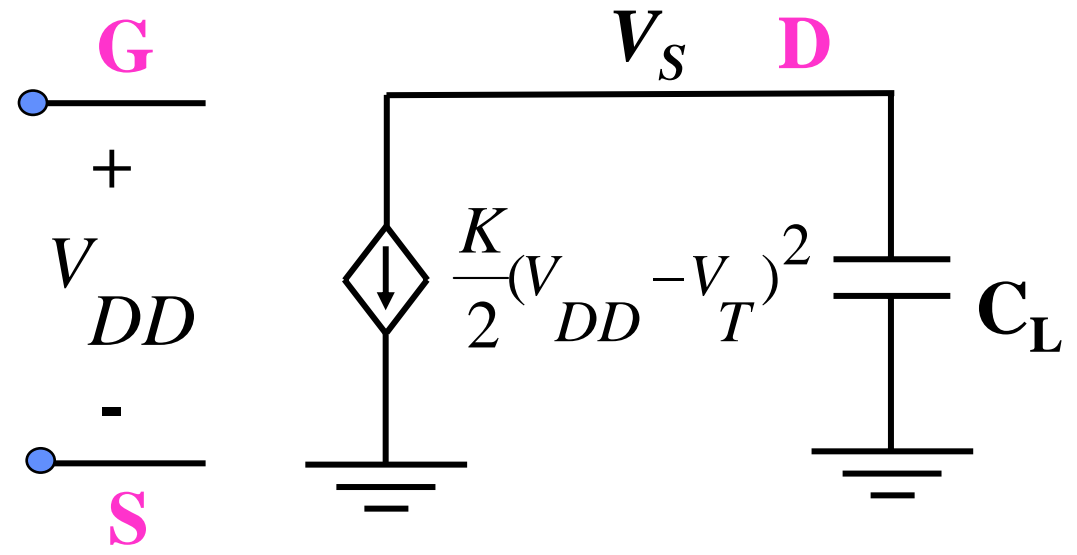## Tree Topology

A   B C   D

$$(A+B) + (C+D)$$

- Balancing paths reduces glitching transitions
- Structures such as multipliers have lot of glitching transitions
- Keeping logic depths short (e.g., pipelining) reduces glitching

V_{DD}

V_{DD}

IN

OUT

t =0+

G

V_S **D**

+

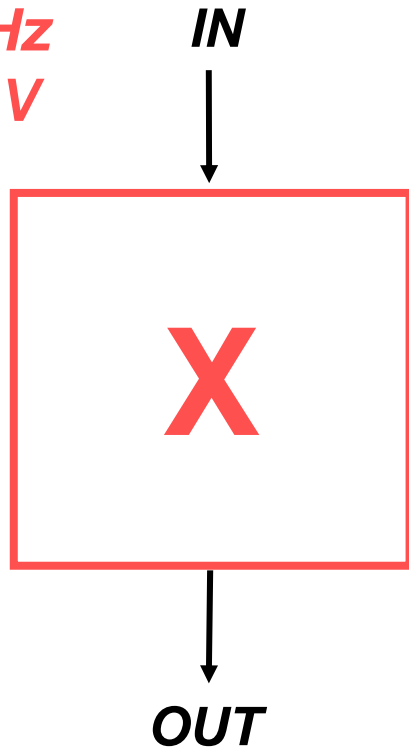V_{DD}

-

S

$\frac{K}{2}(V_{DD} - V_T)^2$

C_L

$$Delay = \frac{C_L \cdot \Delta V}{i_D} = \frac{C_L \cdot \frac{V_{DD}}{2}}{\frac{k}{2}(V_{DD} - V_T)^2} \propto \frac{V_{DD}}{(V_{DD} - V_T)^2} \approx \frac{1}{V_{DD}}$$

V_{DD} from 2V to 1V, energy ↓ by x4, delay ↑ x2

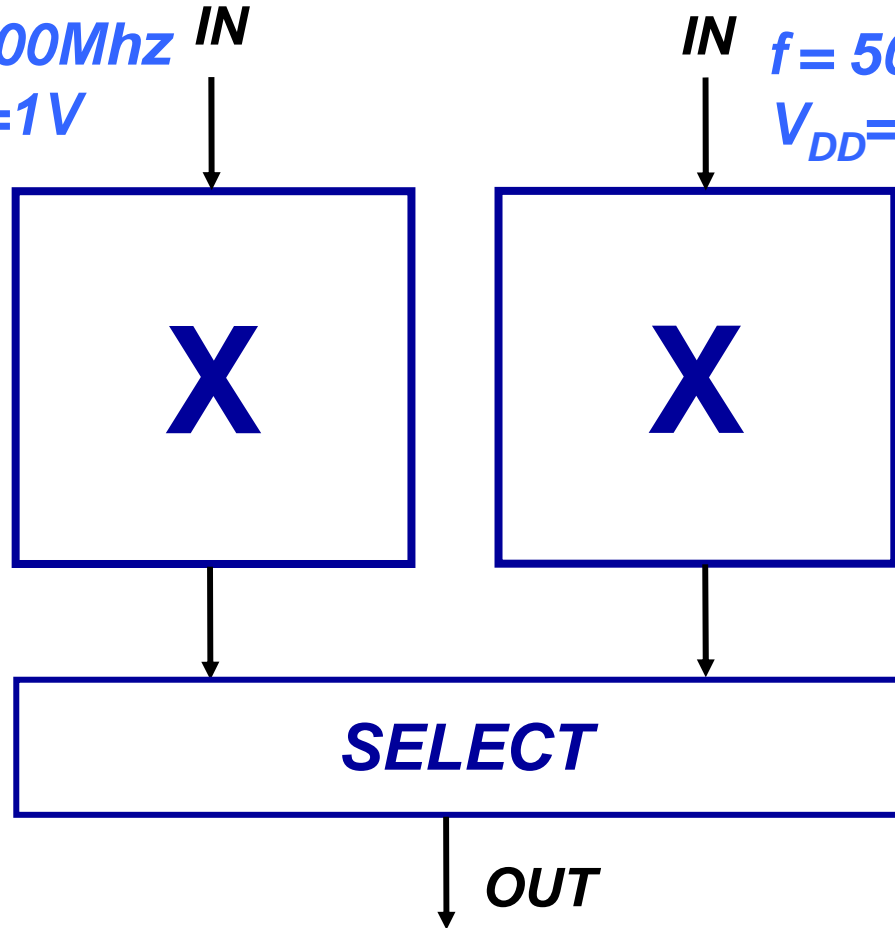# Transistors Are Free…
(What do you do with a Billion Transistors?)

f=1GHz
V_{DD}=2V

IN

X

OUT

$$P_{serial} = C_{mult}\ 2^2\ f$$

f = 500Mhz
V_{DD}=1V

IN

f = 500Mhz
V_{DD}=1V

IN

X

X

SELECT

OUT

$$P_{parallel} = (2C_{mult}\ 1^2\ f / 2) = P_{serial}/4$$

Trade Area for Low Power

Algorithmic Workload

Compare Current Image...

Receiver just updates

...to Previous Image

Frequency of Occurrence

0.06

0.04

0.02

0.00

0   500   1000   1500   2000
Number of IDCTs per Frame
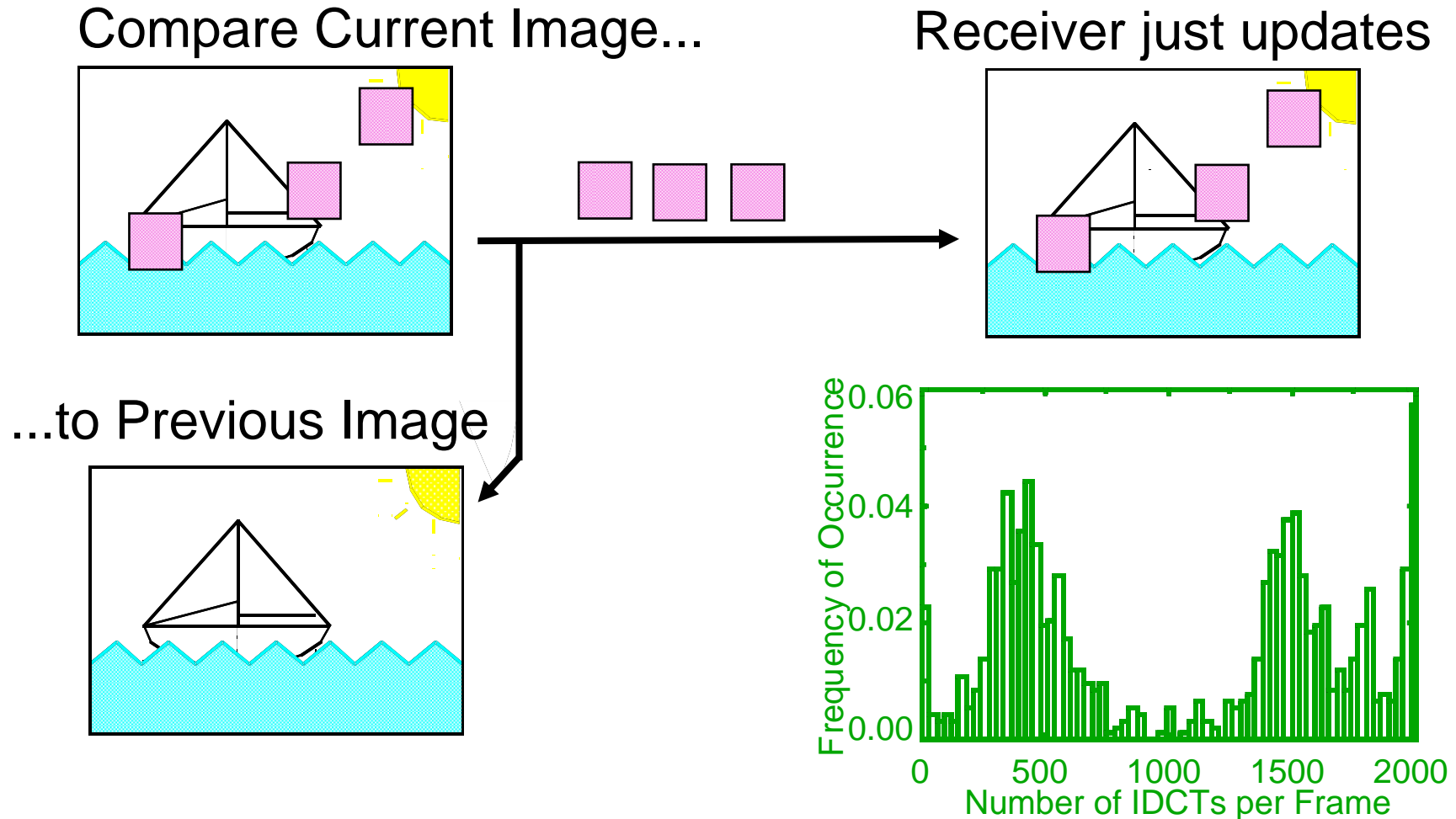
*Exploit Time Varying Algorithmic Workload
To Vary the Power Supply Voltage*

Dynamic Voltage Scaling (DVS)

Fixed Power Supply

ACTIVE	IDLE

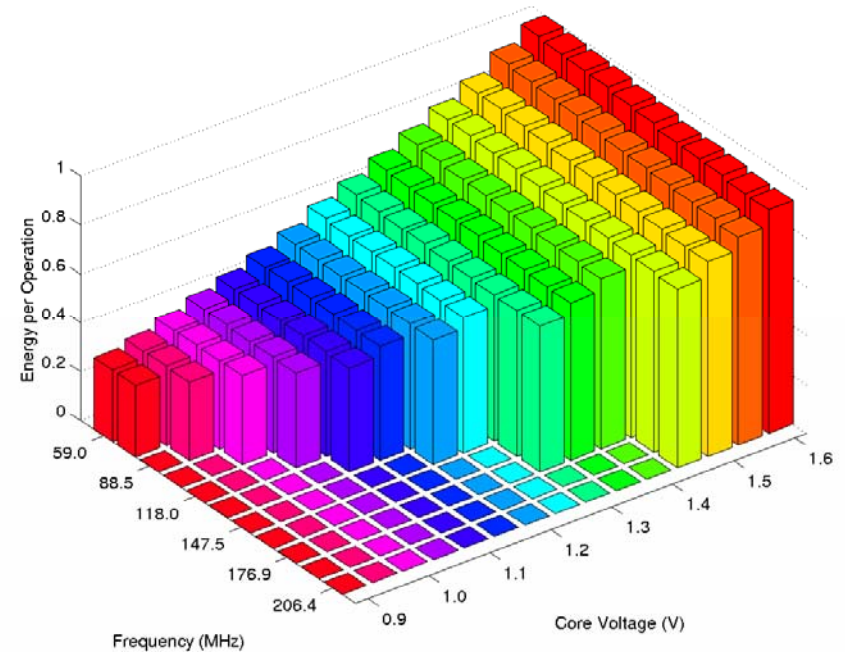$$E_{FIXED} = \tfrac{1}{2} C V_{DD}^2$$

Variable Power Supply

ACTIVE

$$E_{VARIABLE} = \tfrac{1}{2} C (V_{DD}/2)^2 = E_{FIXED} / 4$$

[Gutnik97]

DVS on a Processor
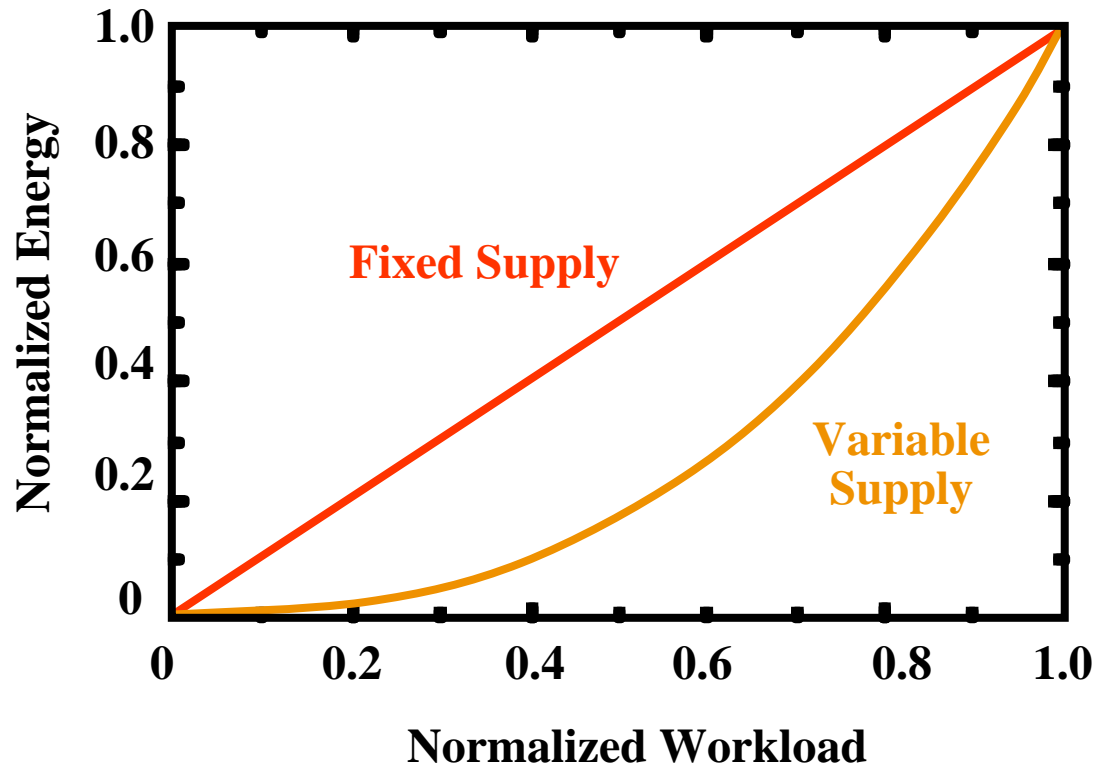
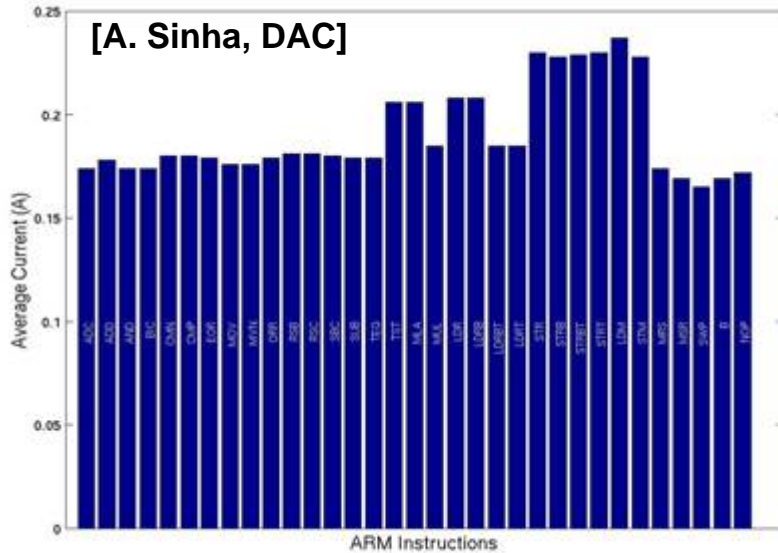**Digitally adjustable DC-DC converter powers SA-1110 core**

Controller

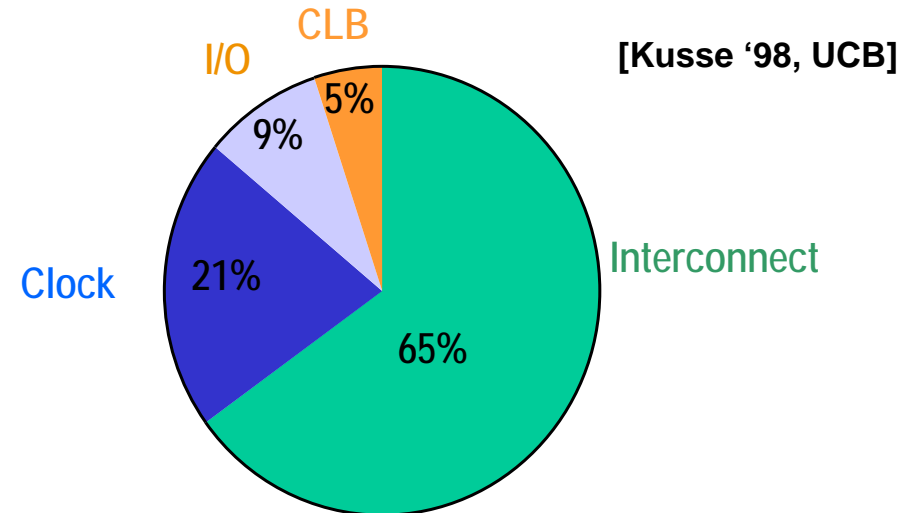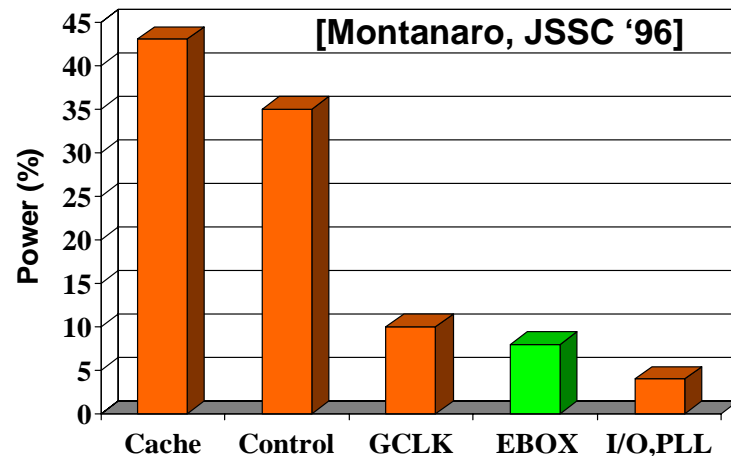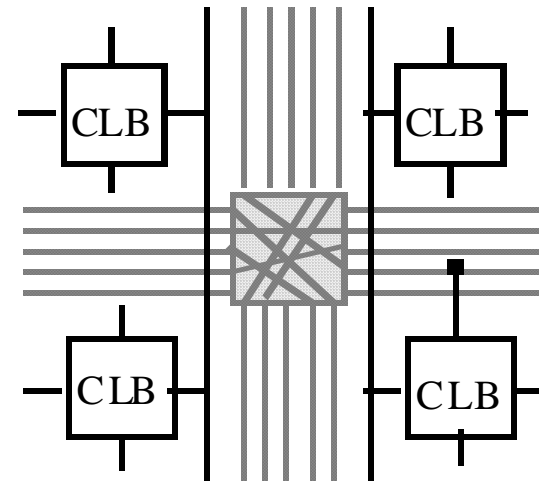**3.6V**

5

V_{out}

SA-1110

Control

μOS
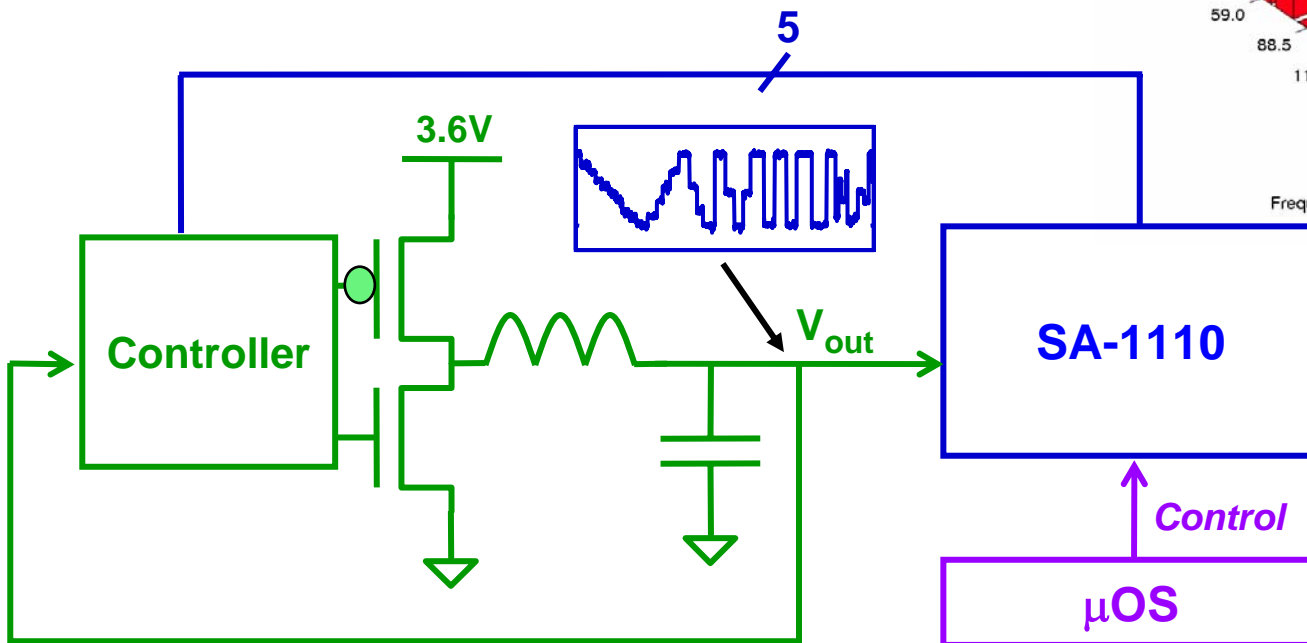
μ**OS selects appropriate clock frequency based on workload and latency constraints**

Hardware vs. Software

Flexibility (vertical axis)

Energy/Operation (horizontal axis)

0.1-1pJ/Op — **Direct Mapped Hardware**

FPGA

0.25nJ/Op — **DSP**

1nJ/Op — **Embedded Processor**

Courtesy of R. Brodersen, J. Rabaey, TI, ARM/StrongARM

Energy Efficiency of Software
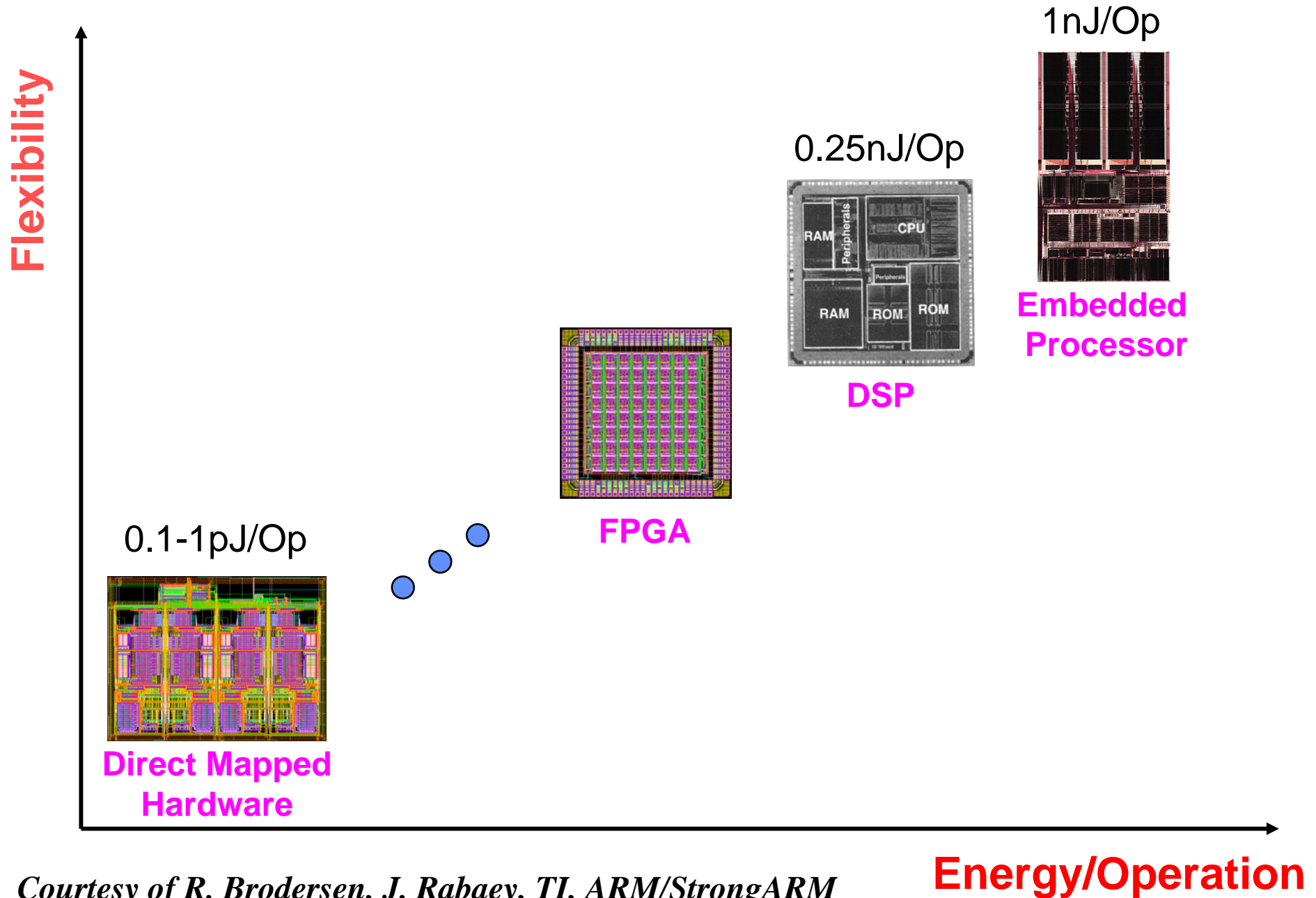
Processor (StrongARM-1100)

[A. Sinha, DAC]

Average Current (A) vs ARM Instructions

[Montanaro, JSSC '96]

Power (%): Cache, Control, GCLK, EBOX, I/O,PLL

FPGA (Xilinx)

CLB   CLB
CLB   CLB

[Kusse '98, UCB]

- CLB 5%
- I/O 9%
- Clock 21%
- Interconnect 65%

"Software" Energy Dissipation has Large Overhead

Trends: Leakage and Power Gating

$$E = CV_{DD}^2$$

$$E = V_{DD}I_0 10^{-V_T/S}$$

Switching (computing)

Leakage (standby)

Total Energy/Switching Energy vs Duty Cycle (%)

Legend: 1.5V, 206MHz; 1.0V, 103MHz

Low V_T devices are leaky - Use a High V_T device is used to gate leakage current

Sleep

Trends: Energy Scavenging
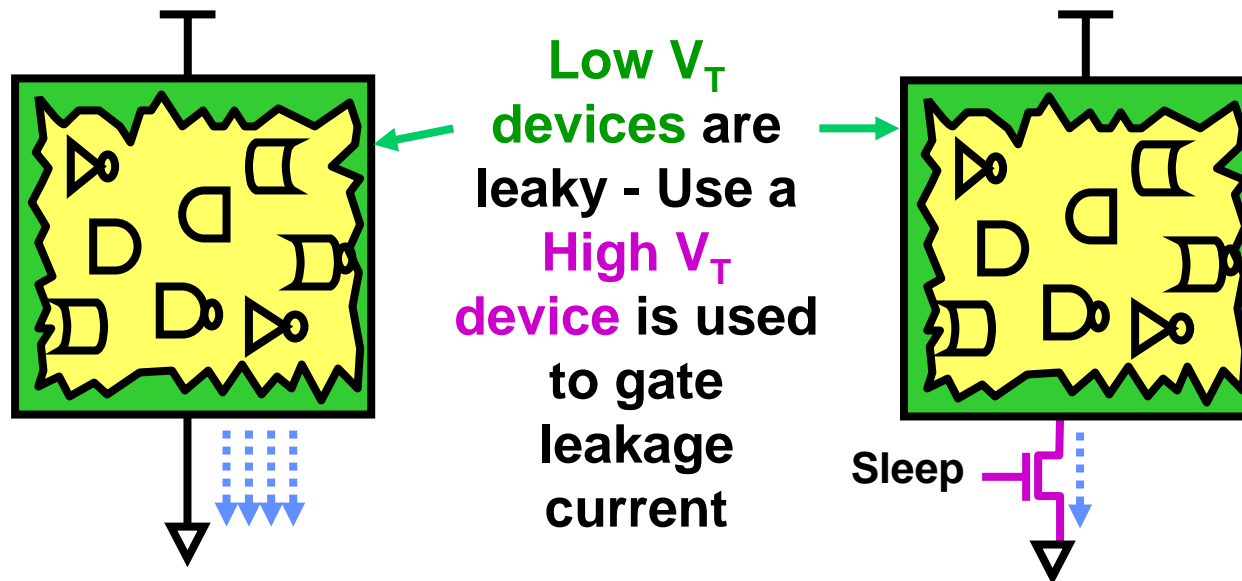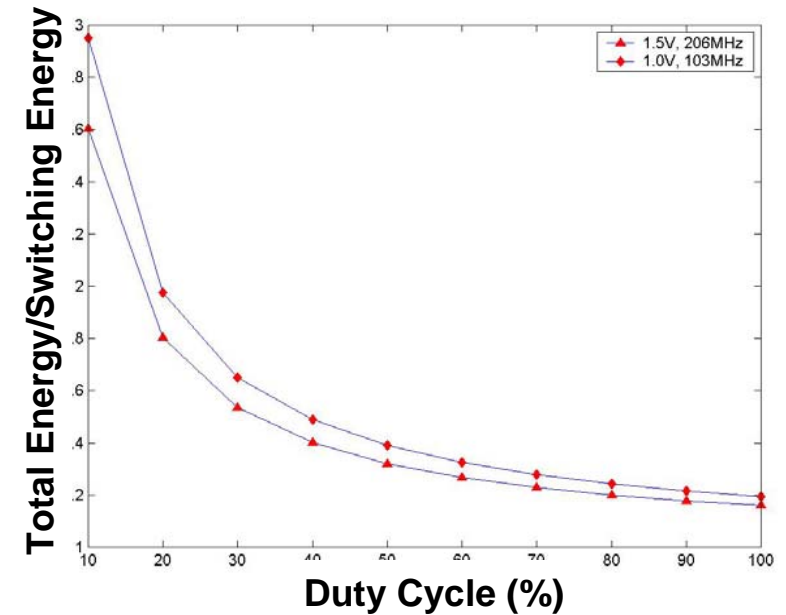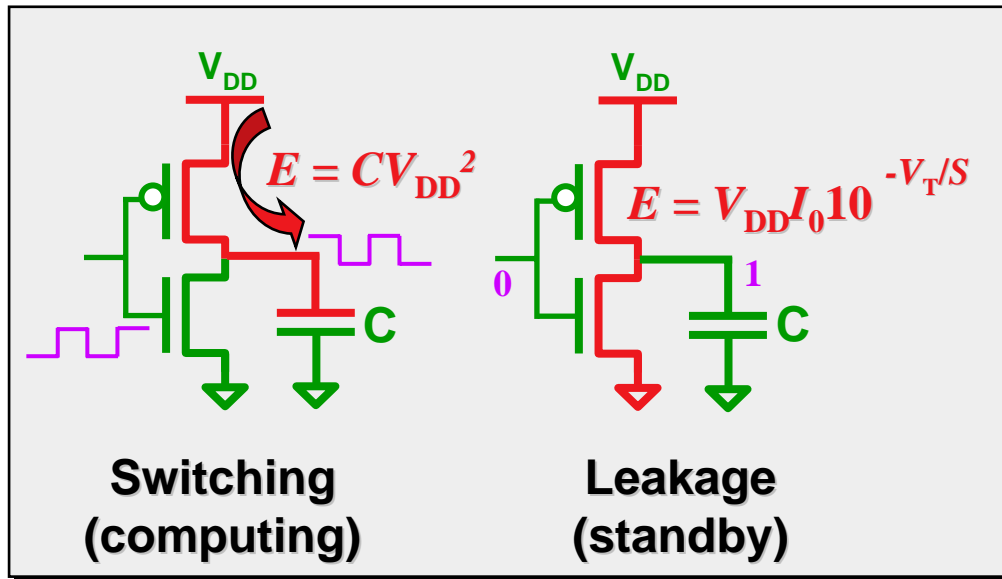
MEMS Generator
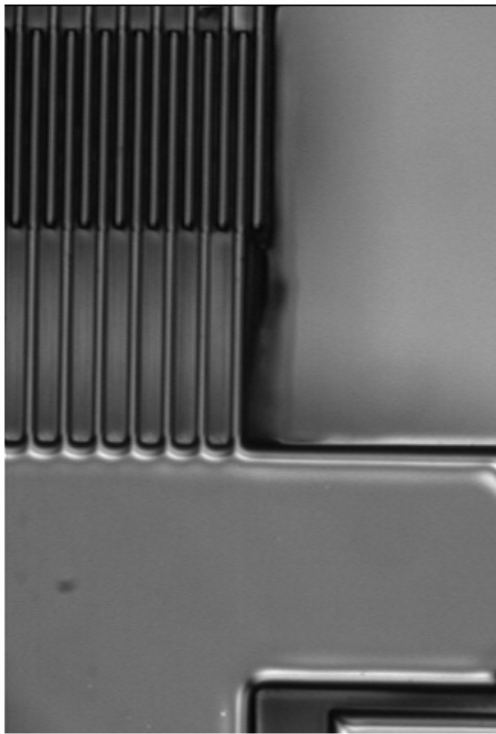
**Jose Mur Miranda/
Jeff Lang**

**Vibration-to-Electric
Conversion**

~ 10μW

Power Harvesting Shoes

**Joe Paradiso
(Media Lab)**

**After 3-6 steps, it provides 3 mA
for 0.5 sec**

~10mW