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An HFT Accelerator

One interesting application of FPGA is high frequency trading (HFT). The goal in this regime is to react as fast as possible to changes in the market. A recent trend in the industry is a move towards FPGAs to minimize the critical path. To that end, we are interested in building a high frequency trading system in FPGA that can parse data from the market using a protocol, envoke logic in our system to react to the update, do risk calculation, and then submit an order back to the market. The goal of the system is to do this in a deterministic and low latency manner. Because FPGAs are resource limited, we might explore using on board CPU to offload more complex operations in the later parts of the project as a stretch goal. We will still have a fast path in our FPGA for reacting to the market by submitting orders bypassing the on board CPU. The high level architecture will preserve a modeling idiom that will yield flexibility within the bypass model to allow system specialization.