6.111 Final Project Checklist
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15 November 2019

Goal	Description	Scheduled Completion Date	Actual Completion Date
LEDs + verilog	Have chess board LED hardware setup + demonstrate verilog capable of individual selection of LEDs + sweep	November 18	
State reading -> 64 bit state signal verilog	Have hall effect sensor + chess piece magnet hardware setup and demonstrate board state occupancy signal construction in verilog	November 20	
communication over UART	Demonstrate successful send and receive of 4 byte from_to signal over UART	November 21	
FSM with move validity checking	Have Verilog track piece types + movements and check validity	December 4	
LED move display	Have verilog construct possible moves on piece lift, then send appropriate signals to LED grid	December 6	
Chess timer w built in 7 set display	Implement a chess timer system in verilog which displays on the 7 segment display	December 9	
VGA display of state	Have verilog push a visual representation of the board, possible moves, and opponent moves to VGA display	December 9	

Red — Minimum Viable Product
Yellow — Complete and Functioning Product
Green — Additionally Featured Product