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FPGA SDR

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Abstract:

For our final project, we will implement the digital end of a software defined radio (SDR) entirely on a FPGA. The minimum viable product will include a view of the received RF spectrum on a VGA display (with bandwidth limited by ADC and RF front end hardware, but at least up to approximately 500 kHz given the 1 MSPS ADC onboard Nexys DDR board). This will be accomplished with a short-time Fourier transform (STFT) of the digitized signal. In addition, users will be able to select a channel (carrier) frequency and demodulate an AM audio signal, which will be output on a speaker. The radio front-end will be simulated with a function generator outputting an AM audio signal. Several digital filters will be included in the design. Additional features to be implemented include FM demodulation with audio output, a waterfall display, and interfacing with a RF front end and high sampling rate ADC to receive live radio broadcasts.