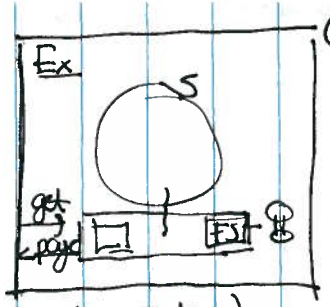
L7 3/4/06
perf
DPi

⑧ Today: performance
~~Techniques~~
Cache
Concurrency
Batchy
Scheduly
} show complexity

① Ex


(show code 1)

② Approach
simple
↓
measure/analyze
↓
adjust design
↑ ↓
done

intrinsic vs. fixed by ~~fixed~~ current tech.

③ Pipeline

$L \geq \sum L_i$
$T = 1/L$

④ (show disk slides)
Disk
$L = S + R + T$
8m 8m 10MB/s
8m/day.
$L(4k) = 8 + 4 + 0.4 = 12.4$
$T(4k) \approx 32$kB. $\neq 10$MB.

+ real disk

⑤ Cache
$A = H \times A_H + (1-H) \times A_m$.
$0.99 \times 10ns + 0.01 \times 10ms$.
100 µs ⇒ 100x !
locality of ref.

(show code + adjust S)
(adjust model

⑥ Replacement
opt
HW

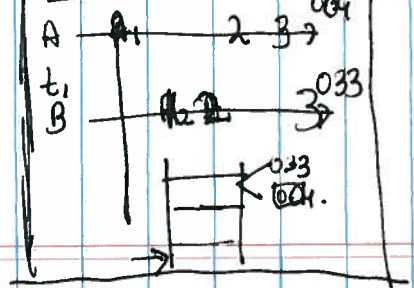
HW: dictated by cache structure
- direct-mapped
- set associative
SW: flexible

⑦ ~~Concurrency~~ Miss

⇒ overlap with threads.

show code 3
+
4.
(adjust picture).

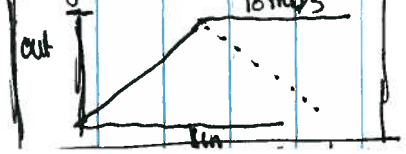
⑧ ~~Recurs~~ ch 6.033
thread
address space
~~process~~

⑨ race


⇒ complexity

⑩ adjust picture
Opportunities: Queue
- Batchy 0.1 1MB/10MB
T(1MB) = 8 + 1MB/no. ≈ 10MS
T
problem: layout (dpi)

⑪ Scheduly 4100 10
FCFS: 4100 10
SSF: 410 100
↳ starved
Elevator:

⑫ Misc
Dallying
Speculation
Interleaving ⇒ Google.

⑬ ~~Pitfall~~ ~~feedback~~ Feedback