Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science
6.012 Electronic Devices and Circuits
Spring 2007

Design Problem - Digital Circuits
3/21/2007
Due: 4/13/2007

0. Before You Begin

This project may be done in groups of two or individually. Each group of two will submit one report. *Read section 13.5.3 of Howe & Sodini.*

1. Introduction

In this design problem, you will design a buffer chain to drive a large capacitive load. This is a common objective in IC design. For example, signals leaving a chip through package leads must often drive large bond-pad capacitances. Similarly, when driving the switches in switching power supplies, a buffer chain is needed to drive the large gate capacitance of the power FETs. For this assignment, we ask you to design a buffer chain to drive a 20pF capacitive load.

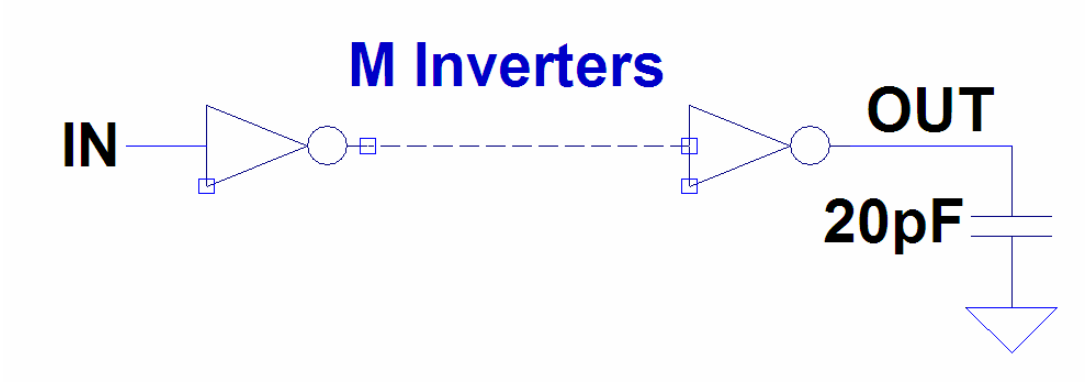

Figure 1: Circuit for Design Problem

With advanced technologies, processing variation in transistor parameters is an added design challenge. For example, processing variations can cause the threshold voltage and channel length to vary from a nominal value. In addition, V_{DD} for the buffer chain is provided by an external power supply, whose output may vary from part-to-part or with temperature. In this project, you will investigate the effect of process and supply variations on propagation delay, power dissipation, and noise margins.

2. Design Methodology

We suggest the following design methodology for this design problem. First, perform enough hand calculations using nominal process parameters and supply voltage to understand the particular challenges of this design problem. Use the hand calculations to gain a feel for effectiveness of the various "knobs" at your disposal (sizing, number of inverters, etc). While doing hand calculations, use the approximate methods given in *Howe and Sodini* to find the noise margins, propagation delays, and power dissipation. For example, when calculating propagation delay, assume that the transistors remain in their constant-current region throughout the transitions, as presented in class.

Once you feel that you understand the design problem, design your circuit to meet specifications using the nominal process parameters and supply voltage. With your design in place, check the various worst-case process corners to see whether you still fall within specification. For example, a particular set of process and supply variations will yield the slowest circuit, while another set of variations will yield a circuit that dissipates the most power. You must test whether you still meet the timing, noise margin, and power specifications when operating under these types of variations.

If your design fails any of the specifications on a particular process corner, then use the understanding gained from hand analysis to iteratively tweak your design until you meet specifications over all process and supply variations.

3. Design Objectives

The design goals in order of importance are: (1) to meet timing constraint over all process corners with a maximum power dissipation of 800uW, (2) to perform the correct logical function with minimum noise margin of 0.45V over all process variations, (3) to minimize power dissipation.

- The propagation delay between IN and OUT must be less than 27 ns (t_{pdLH} and $t_{pdHL} < 27$ns).
- Average power dissipation when the standard input waveform is applied must be less than 800uW.
- All logic gates you design must have noise margins of at least 0.45V.
- The first inverter in the buffer chain must be minimum sized (W_N=6um, W_P=12um, L=1.5um).
- Your circuit model and simulation results must reflect the effects of parasitic capacitances. You need to provide SPICE with information that allows it to calculate parasitic capacitances as described in the following section.
- Once you have met your timing, noise margin, and power dissipation specifications, minimize the power dissipation while still meeting specifications over all process and supply variations.

You must meet the above constraints by sizing the transistors appropriately. Sizes may be specified to the nearest half micron, therefore a width of 8.34µm is not acceptable, but 8.5µm is. The minimum size transistor is (W/L)=(6µm/1.5µm).

Turn in SPICE results and netlists showing that you meet all the design goals using nominal process parameters and supply voltage. Identify which sets of process and supply variations will lead to the slowest circuit, the circuit that dissipates the most power, and the circuit with the smallest noise margins. Turn in SPICE results and netlists showing that you meet the design goals even under these worst-case sets of variations.

4. Specifications

The signal IN is a 50% duty cycle square wave with low value of 0V and high value equal to V_{DD}. The square wave has a frequency of 10MHz, and finite rise and fall times of 2ns. A diagram of the standard input waveform is given as Figure 2. The buffer chain must be structured such that OUT has the same logic value as IN.

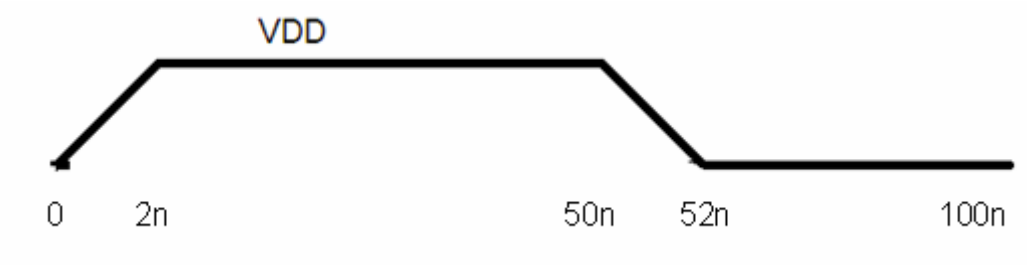

Figure 2: Standard Input Waveform

The minimum dimensions for transistors are W=6um and L=1.5um. The nominal threshold voltages are V_{Tn}= 0.5 V and V_{Tp}= -0.5 V. The oxide thickness is fixed at 15 nm. The mobility is μ_n=220 (cm^2/Vs) for the n-channel device and μ_p=110 (cm^2/Vs) for the p-channel device. Typical numbers for the junction capacitance (CJ), sidewall junction capacitance (CJSW), and the built in potential ØB (PB) have also been calculated and are included in the device models. The parameter LAMBDA=100 mV^{-1} for 1.5µm long devices. When using lengths other than 1.5µm, it is necessary to adjust the value of λ. For a MOSFET of length L, the new λ value is (1.5/L)*100 mV^{-1}. This is because λ is proportional to (1/L). For your convenience, we have created sub-circuit models which are simply a MOSFET but have the λ value and geometries computed for you. Also, the backgate is tied to GND for N-MOSFETS, and VDD for P-MOSFETS. The next section contains information on calculating the AD, AS, PD, and PS parameters.

```
.subckt NFET VDD GND D G S wg=6u lg=1.5u
.model NCH NMOS LEVEL=1 VTO=0.5 TOX=1.5E-8 U0=220
+ LAMBDA='(1.5u/lg)*1.0E-1' CJ=1.0E-4
+ CJSW=5.0E-10 PB=0.95 GAMMA=0.6
M1 D G S GND NCH l='lg' w='wg' ps='12u+wg'
+ pd='12u+wg' as='6u*wg' ad='6u*wg'
.ends NFET

.subckt PFET VDD GND D G S wg=6u lg=1.5u
.model PCH PMOS LEVEL=1 VTO=-0.5 TOX=1.5E-8 U0=110
+ LAMBDA='(1.5u/lg)*1.0E-1' CJ=3.0E-4
+ CJSW=3.5E-10 PB=0.9 GAMMA=0.6
M1 D G S VDD PCH l='lg' w='wg' ps='12u+wg'
+ pd='12u+wg' as='6u*wg' ad='6u*wg'
.ends PFET
```

An example of how to use these models is given with a basic inverter:

```
X1 VDD GND out in VDD PFET wg=12u lg=1.5u
X2 VDD GND out in GND NFET wg=6u  lg=1.5u
```

We ask you to investigate the effect of V_T, channel length, and V_{DD} variation in your circuit. These parameters vary as follows:

Parameter	Nominal Value	Variation
V_{Tn}, $-V_{Tp}$	0.5V	±0.15V
V_{DD}	1.5V	±0.15V
L_N, L_P	1.5um	±0.25um

When checking whether your design meets timing, power dissipation, and noise margin specifications over all process corners, note that the variations between NMOS and PMOS can be independent. For example, processing variations can lead to a V_{Tn}=0.65V and V_{Tp}=-0.35V, or an NMOS length of 1.25um and a PMOS length of 1.75um. However, all the NMOS in your circuit experience the same variations, and all the PMOS in your circuit experience the same variations. For example, if you have two minimum-sized inverters, process variation cannot lead to the NMOS in the first inverter having length of 1.25um and the second inverter having length of 1.75um.

5. Preliminary Design and Calculations

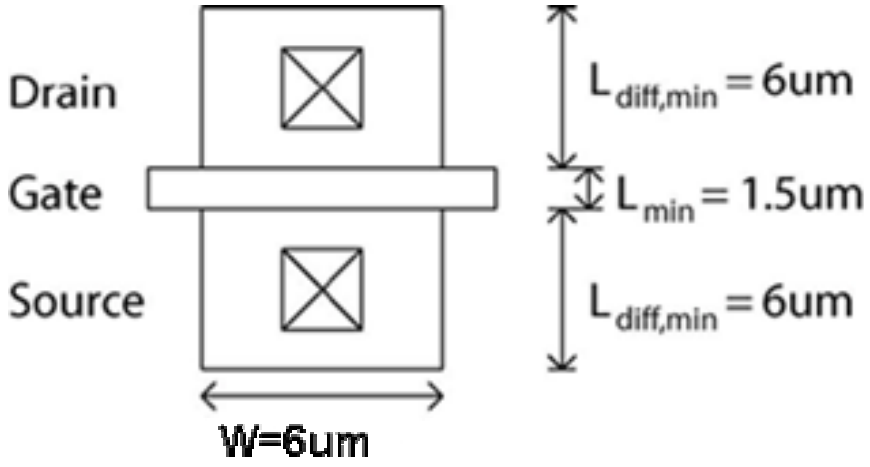

Figure 3: Transistor Layout

In your hand-calculations, you will try to accurately predict the propagation delay and power dissipation of your circuit. To do this, you will need to find the capacitances associated with the transistors, which requires some knowledge of transistor layout.

A simple transistor layout is shown in Figure 3, which shows the minimum size device you may use for this project. The minimum gate length is 1.5 µm and the gate width is 6µm. In order to contact the source and drain, we must leave a 2 micron space for the contact itself and 2 microns on either side as overlap, to ensure that the contact hole is over only the diffused area, and not the surrounding bulk silicon. Any of these dimensions may be bigger, but it is not advantageous to make the source or drain bigger, since it only adds to the parasitic capacitance.

The parasitic capacitance arises because there is a p-n junction between the source or drain region and the substrate. This junction should remain reverse biased, so we need only worry about depletion capacitance. There are two capacitance parameters in the model statements above, CJ and CJSW. CJ (units: F/m^2) is the capacitance per unit area of the bottom of the source or drain region. You specify the area of the source or drain in the description of the individual transistor. CJSW (units: F/m) is the capacitance of the

"sidewall," or perimeter, of the source or drain region. It is specified as a capacitance per unit length because the other dimension, depth, is a parameter of the process, not controllable by the circuit designer. Again, you specify the perimeter of the source and drains in the description of the transistor. The capacitances calculated from CJ and CJSW are the zero voltage capacitances of the p-n junctions.
As an example, let us find the area and SPICE description for the above transistor. The gate length is 1.5 μm and the gate width is 6 μm. The perimeters of the source and drain are 6 + 6 + 6 = 18 μm, since the side near the gate is accounted for in the gate capacitance. The areas are 6 x 6 = 36 $(\mu m)^2$ = 36 x $10^{-12}m^2$. Notice that these are specified with a "p" for 10^{-12} in the SPICE input. The area of the gate region is 1.5 x 6 = 9 x $10^{-12}m^2$. The total area of the transistor is thus 36 + 36 + 9 = 81 square microns.

Below is a typical SPICE description of our minimum size transistor.

```
m1 1 2 3 4 n15 L=1.5u W=6u ps=18u pd=18u as=36p ad=36p
```

You must hand calculate the parasitic drain-substrate and gate-source capacitance for your transistors, as they can have a significant effect on the speed and power dissipation of the circuit. To simplify your hand calculations, assume that the capacitors are linear with value equal to the zero voltage capacitance. This will produce a conservative design, as the average capacitance is less than the zero voltage capacitance.

6. HSPICE Simulation

You will need to do two different kinds of simulations: DC sweeps and transients. The DC sweep is used to find the voltage transfer functions of various stages. The easiest way to run DC sweeps is to create an HSPICE deck that contains transistor models, the sub-circuit under test, and simulation commands. Awaves can plot the input voltage on the x-axis, and the output voltage on the y-axis.

Use a transient simulation to measure propagation delays. The delay times for CMOS logic circuits are defined as the period from one signal crossing $V_{DD}/2$ to a second signal crossing $V_{DD}/2$. For accuracy, please use a timescale of 1ps in your transient simulation.

To measure power dissipation, integrate the current out of the V_{DD} voltage source over one period of the standard input waveform. Awaves has an expression builder that allows you to plot functions of circuit voltages and currents. To integrate the current from V_{DD}, create the expression:

```
integral(node(D0,"A0","i(vdd)"))
```

Note: To create this expression, you will have to drag the `i(vdd)` object from the "Results Browser" into the "Expression Builder" using the **middle-click** button on your mouse.

Average power dissipation is given by the formula below, where ***T=100ns***.

$$P_{Diss} = \frac{1}{T}\int_0^T (I \bullet V_{DD})dt$$

Use a DC sweep to measure the noise margins. Awaves can report the derivative of the voltage transfer function at V_M. Use the straight-line approximations given in *Howe & Sodini* to find V_{IL} and V_{IH}.

6. Report

Your group will write a report detailing your design efforts. Be clear and concise. The following must be included in the report:

1. An explanation of the approach you took to arrive at the design for nominal process parameters, in one page or less. What steps did you take to create the correct logical function, meet timing requirements, and meet power dissipation? This section is very important.
2. What approach did you use to minimize the power?
3. A transistor-level schematic diagram that shows transistor sizes (W and L) and how they are connected.
4. Summarize your hand calculations. Show how you chose the number of inverters in the buffer chain and the size of each transistor. Show approximate calculations for the expected propagation delays t_{pdLH} and t_{pdHL}, and for power dissipation for the standard input waveforms. What part(s) of the circuit dissipate the most power?
5. Fill in the summary form with the appropriate hand-calculated and simulated values for your circuit.
6. Include waveform plots from Awaves for nominal process parameters and supply voltage that illustrate:
    a. the noise margins for the largest inverter in the buffer chain
    b. the propagation delays from IN to OUT
7. Analyze the impact of process and supply variations on your circuit:
    a. Identify which process and supply variations $\{V_{DD}, V_{TN}, V_{TP}, L_N, L_P\}$ lead to the slowest design.
    b. Identify which process and supply variations $\{V_{DD}, V_{TN}, V_{TP}, L_N, L_P\}$ lead to the design that dissipates the most power.
    c. Identify which process and supply variations $\{V_{DD}, V_{TN}, V_{TP}, L_N, L_P\}$ lead to the smallest noise margins.
    d. Include waveform plots from Awaves that illustrate that these variations do lead to the slowest design, the design that dissipates the most power, and the design with the smallest noise margins.
    e. Explain why these particular variations lead to the slowest design, the design that dissipates the most power, and the design with the smallest noise margins. The explanation is very important.
8. Put your HSPICE file(s) in a publicly readable directory in your Athena account, so that we may copy them and run our own simulations of your circuit. Your "Public" directory is a good location. Write your username and the directory in the space on the summary page. Please create 5 spice files named as follows:
    a. Nominal-tran.sp should contain a transient simulation using nominal process parameters and supply voltage.
    b. Nominal-dc.sp should contain a DC sweep using nominal process parameters and supply voltage.
    c. Worst-tpd.sp should contain a transient simulation using the set of process parameters and supply voltage that yielded the slowest design.
    d. Worst-pdiss.sp should contain a transient simulation using the set of process parameters and supply voltage that yielded the design that dissipated the most power.
    e. Worst-nm.sp should contain a DC sweep using the set of process parameters and supply voltage that yielded the design with the worst noise margins for the largest inverter.

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Design Problem #1 - Digital Circuits

Name(s):_____

Athena username(s):_____

Recitation Section(s):_____

Performance Specifications over Nominal Process Parameters and Supply Voltage

Parameter	Specification	Calculated value	Simulated value
t_{pdLH}	<27ns		
t_{pdHL}	<27ns		
Average Power Dissipation for Standard Input	<800uW		
NM_H (for Largest Inverter)	0.45V		
NM_L (for Largest Inverter)	0.45V		

Performance Specifications over Worst-Case Process Parameters and Supply Voltage

Parameter	Specification	Process Parameters and Supply Voltages	Simulated value
Worst-Case t_{pdLH}	<27ns	V_{DD}: V_{TN}: V_{TP}: L_N: L_P:	
Worst-Case t_{pdHL}	<27ns	V_{DD}: V_{TN}: V_{TP}: L_N: L_P:	
Worst-Case Power Dissipation	<800uW	V_{DD}: V_{TN}: V_{TP}: L_N: L_P:	
Worst-Case NM_H	0.45V	V_{DD}: V_{TN}: V_{TP}: L_N: L_P:	
Worst-Case NM_L	0.45V	V_{DD}: V_{TN}: V_{TP}: L_N: L_P:	