Lecture 7

PN Junction and MOS Electrostatics(IV)

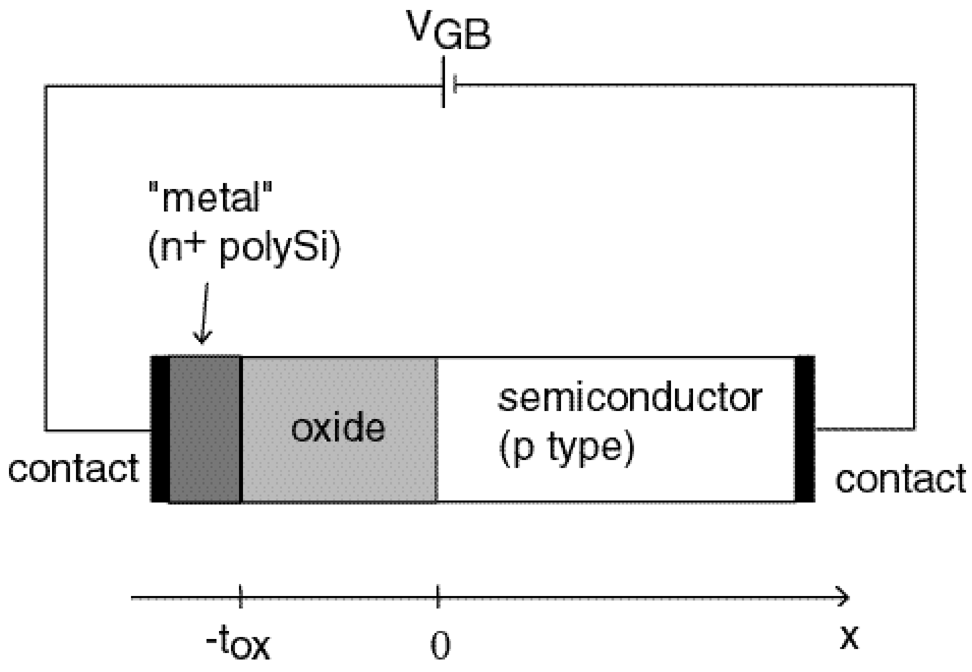
<u>M</u>etal-<u>O</u>xide-<u>S</u>emiconductor Structure (contd.)

Outline

1. Overview of MOS electrostatics under bias
2. Depletion regime
3. Flatband
4. Accumulation regime
5. Threshold
6. Inversion regime

Reading Assignment:
Howe and Sodini, Chapter 3, Sections 3.8-3.9

1. Overview of MOS electrostatics under bias



Application of bias:

- Built-in potential across MOS structure increases from ϕ_B to $\phi_B + V_{GB}$
- Oxide forbids current flow ⇒
  - J=0 everywhere in semiconductor
  - Need **drift = -diffusion** in SCR
- Must maintain boundary condition at Si/SiO$_2$ interface
  - $E_{ox} / E_s \approx 3$

How can this be accommodated simultaneously? ⇒ ***quasi-equilibrium situation*** with potential build-up across MOS equal to $\phi_B + V_{GB}$

Important consequence of quasi-equilibrium:

⇒ Boltzmann relations apply in semiconductor

[they were derived starting from $J_n = J_p = 0$]

$$n(x) = n_i e^{q\phi(x)/kT}$$

$$p(x) = n_i e^{-q\phi(x)/kT}$$

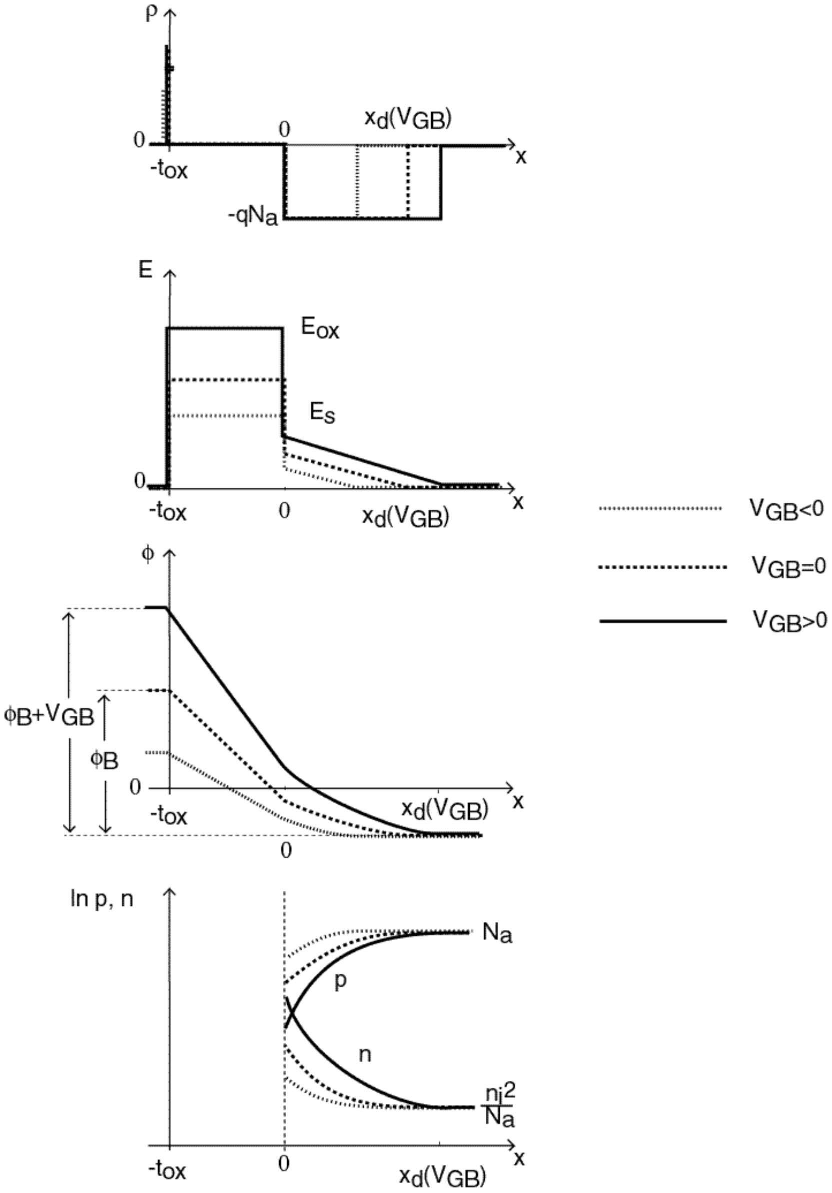
and

$$np = n_i^2 \qquad \text{at every x}$$

2. Depletion regime

For $V_{GB}>0$, metal attracts electrons and repels holes
⇒ ***Depletion region widens***

For $V_{GB}<0$, metal repels electrons and attracts holes
⇒ ***Depletion region shrinks***



In depletion regime, all results obtained for thermal equilibrium apply if $\phi_B \rightarrow \phi_B + V_{GB}$.

For example:

Depletion region thickness:

$$x_d(V_{GB}) = \frac{\varepsilon_s}{C_{ox}} \left[\sqrt{1 + \frac{2C_{ox}^2(\phi_B + V_{GB})}{\varepsilon_s q N_a}} - 1 \right]$$

Potential drop across semiconductor SCR:

$$V_B(V_{GB}) = \frac{q N_a x_d^2}{2\varepsilon_s}$$

Surface potential

$$\phi(0) = \phi_p + V_B(V_{GB})$$

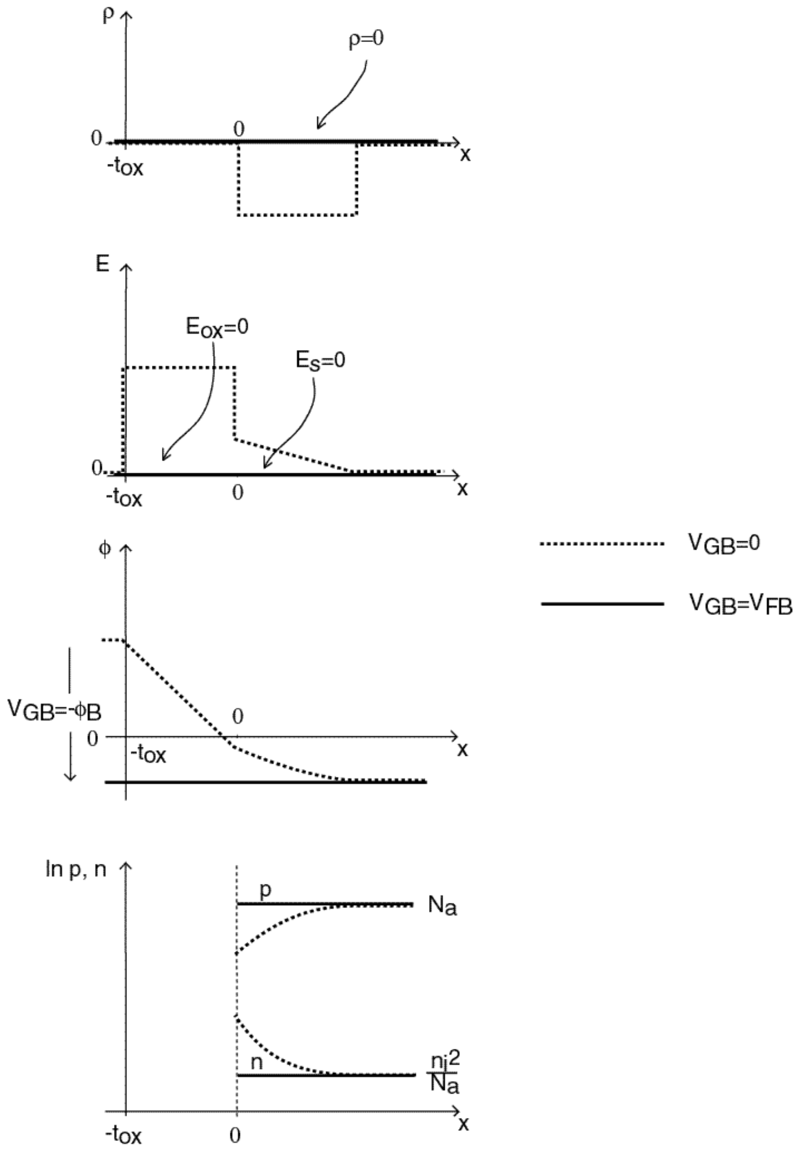
Potential drop across oxide:

$$V_{ox}(V_{GB}) = \frac{q N_a x_d t_{ox}}{\varepsilon_{ox}}$$

3. Flatband

At a certain negative V_{GB}, depletion region is wiped out

$\Rightarrow$ ***Flatband***

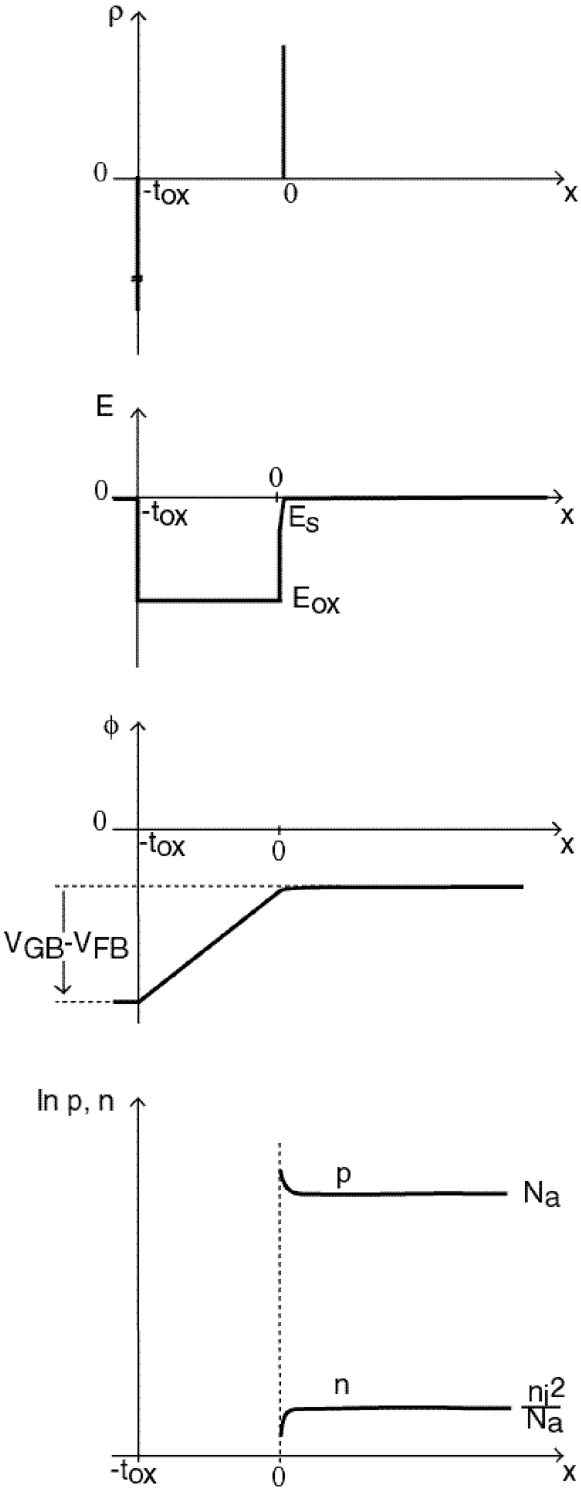


Flatband Voltage:

$$V_{GB} = V_{FB} = -\phi_B = -(\phi_{N^+} - \phi_p)$$

4. Accumulation regime

If $V_{GB} < V_{FB}$ accumulation of holes at Si/SiO$_2$ interface

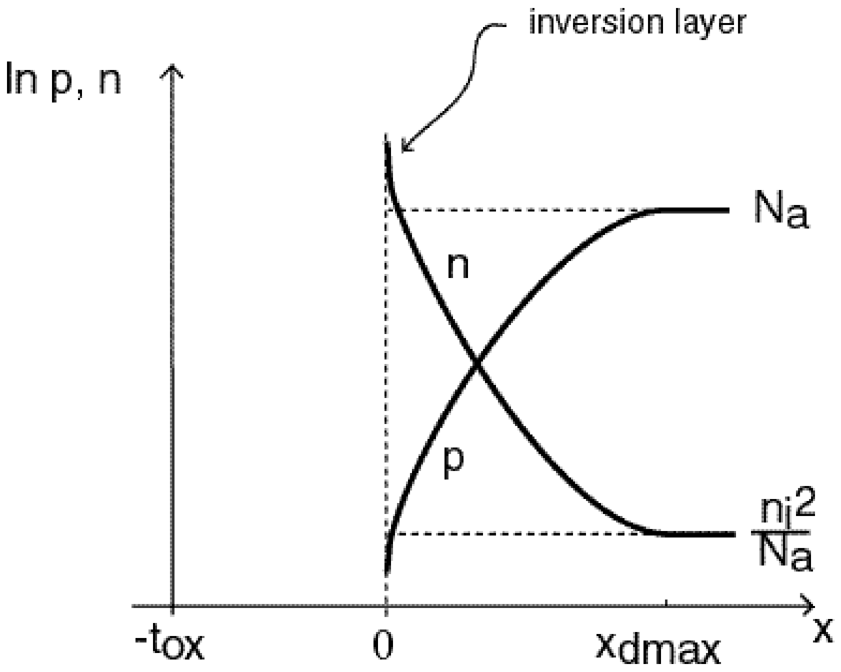


5. Threshold

Back to $V_{GB}>0$.

For sufficiently large $V_{GB}>0$, electrostatics change when $n(0)=N_a \Rightarrow$ ***threshold***.

Beyond ***threshold***, we **cannot** neglect contributions of electrons towards electrostatics.



Let's compute the gate voltage (***threshold voltage***) that leads to $n(0)=N_a$.

Key assumption: use electrostatics of depletion (neglect electron concentration at threshold)

Computation of threshold voltage.

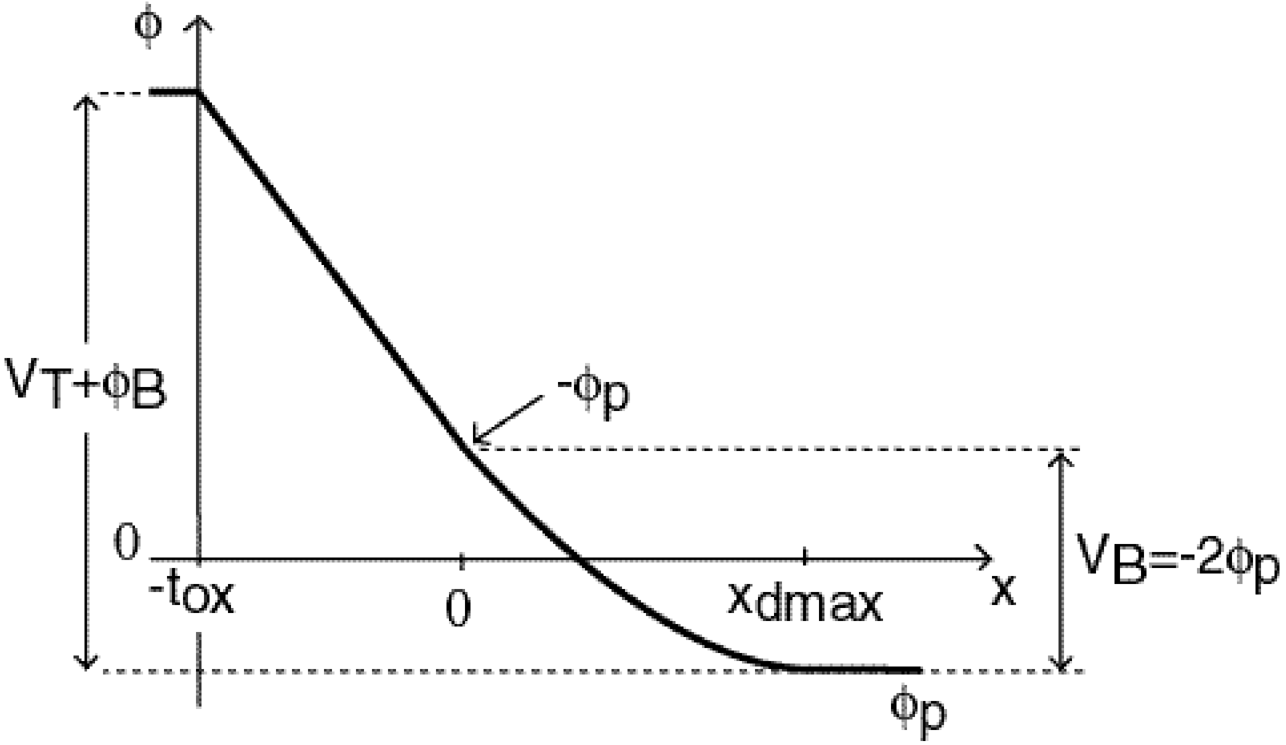
Three step process:

First, compute potential drop in semiconductor at threshold. Start from:

$$n(0) = n_i e^{q\phi(o)/kT}$$

Solve for $\phi(0)$ at $V_{GB} = V_T$:

$$\phi(0)\Big|_{V_{GB}=V_T} = \frac{kT}{q} \bullet \ln \frac{n(0)}{n_i}\Bigg|_{V_{GB}=V_T} = \frac{kT}{q} \bullet \ln \frac{N_a}{n_i} = -\phi_p$$



Hence:

$$V_B(V_T) = -2\phi_p$$

Computation of threshold voltage (contd.)

Second, compute potential drop in oxide at threshold.

Obtain $x_d(V_T)$ using relationship between V_B and x_d in depletion:

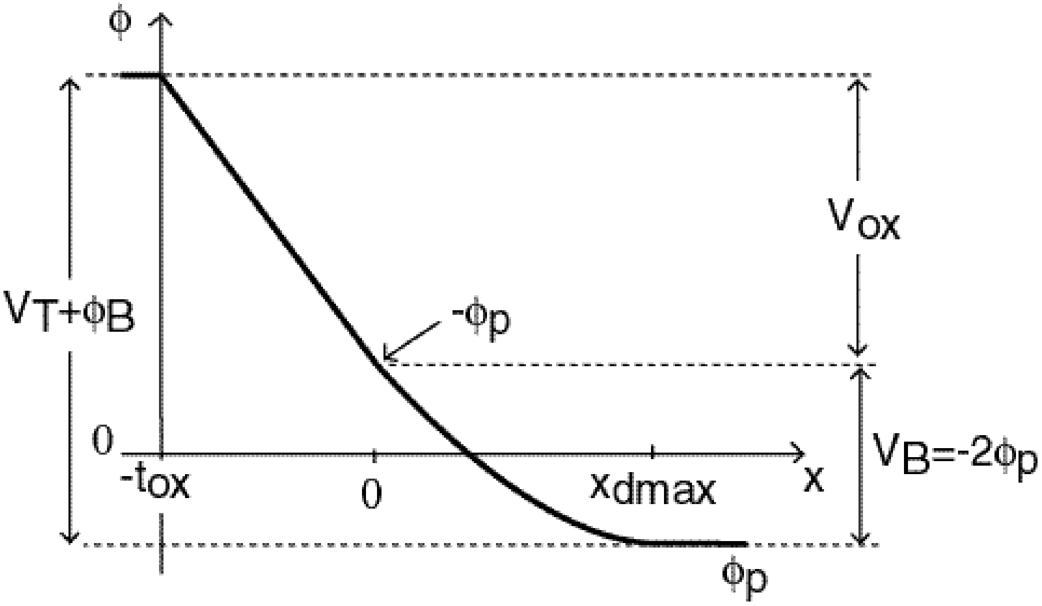
$$V_B(V_{GB} = V_T) = \frac{qN_a x_d^2(V_T)}{2\varepsilon_s} = -2\phi_p$$

Solve for x_d at $V_{GB} = V_T$:

$$x_d(V_T) = x_{d\max} = \sqrt{\frac{2\varepsilon_s(-2\phi_p)}{qN_a}}$$

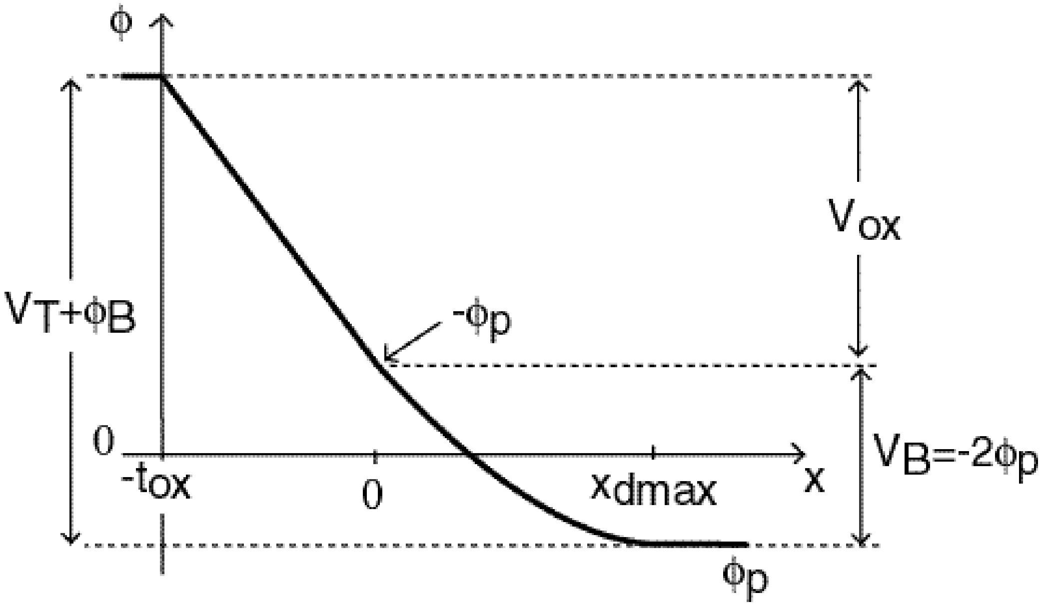
Then:

$$V_{ox}(V_T) = E_{ox}(V_T)t_{ox} = \frac{qN_a x_d(V_T)}{\varepsilon_{ox}} t_{ox} = \frac{1}{C_{ox}}\sqrt{2\varepsilon_s qN_a(-2\phi_p)}$$



Computation of threshold voltage. (contd..)

Finally, sum potential drops across structure.



$$V_T + \phi_B = V_B(V_T) + V_{ox}(V_T) = -2\phi_P + \frac{1}{C_{ox}}\sqrt{2\varepsilon_s q N_a(-2\phi_p)}$$

Solve for V_T:

$$V_{GB} = V_T = V_{FB} - 2\phi_P + \frac{1}{C_{ox}}\sqrt{2\varepsilon_s q N_a(-2\phi_p)}$$

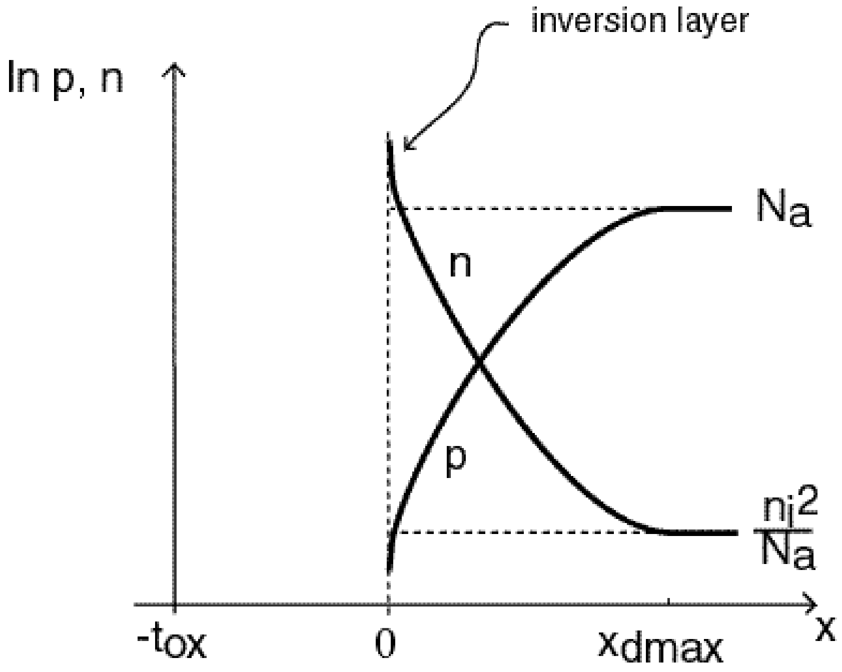
Key dependencies:

- **If N_a ↑ ⇒ V_T ↑**. The higher the doping, the more voltage required to produce $n(0) = N_a$
- **If C_{ox} ↑ (t_{ox}↓) ⇒ V_T ↓**. The thinner the oxide, the less voltage dropped across the oxide.

6. Inversion

What happens for $V_{GB} > V_T$?

More electrons at Si/SiO_2 interface than acceptors
⇒ ***inversion.***



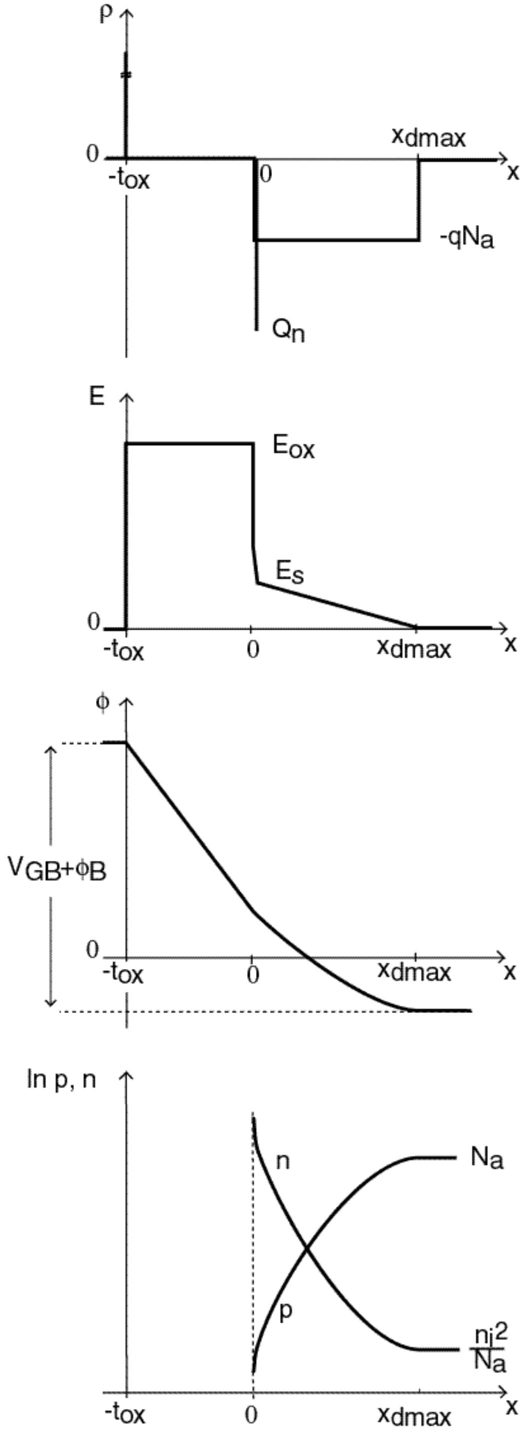
Electron concentration at Si/SiO_2 interface modulated by $V_{GB} \Rightarrow V_{GB} \uparrow \rightarrow n(0) \uparrow \rightarrow |Q_n| \uparrow$:
Field-effect control of mobile charge density!
[essence of MOSFET]

Want to compute Q_n vs. V_{GB} [***charge-control relation***]

Make ***sheet charge approximation***: electron layer at Si/SiO_2 is much thinner than any other dimension in problem (t_{ox}, x_d).

Charge-Control Relation

To derive the charge-control relation, let’s look at the overall electrostatics:



Charge-Control Relation (contd.)

Key realization:

$$n(0) \propto e^{q\phi(0)/kT}$$

$$qN_a x_d \propto \sqrt{\phi(0)}$$

Hence, as V_{GB} ↑ and $\phi(0)$ ↑ , n(0) will change a lot, but $|Q_d|$ will change very little.

Several consequences:

- x_d does not increase much beyond threshold:

$$x_d(inv.) \approx x_d(V_T) = \sqrt{\frac{2\varepsilon_s(-2\phi_p)}{qN_a}} = x_{d,\max}$$

- V_B does not increase much beyond $V_B(V_T) = -2\phi_P$ (*a thin sheet of electrons does not contribute much to* V_B.):

$$V_B(inv.) \approx V_B(V_T) = -2\phi_P$$

Charge-Control Relation (contd..)

- All extra voltage beyond V_T used to increase inversion charge Q_n. Think of it as capacitor:
  - Top plate: metal gate
  - Bottom plate: inversion layer

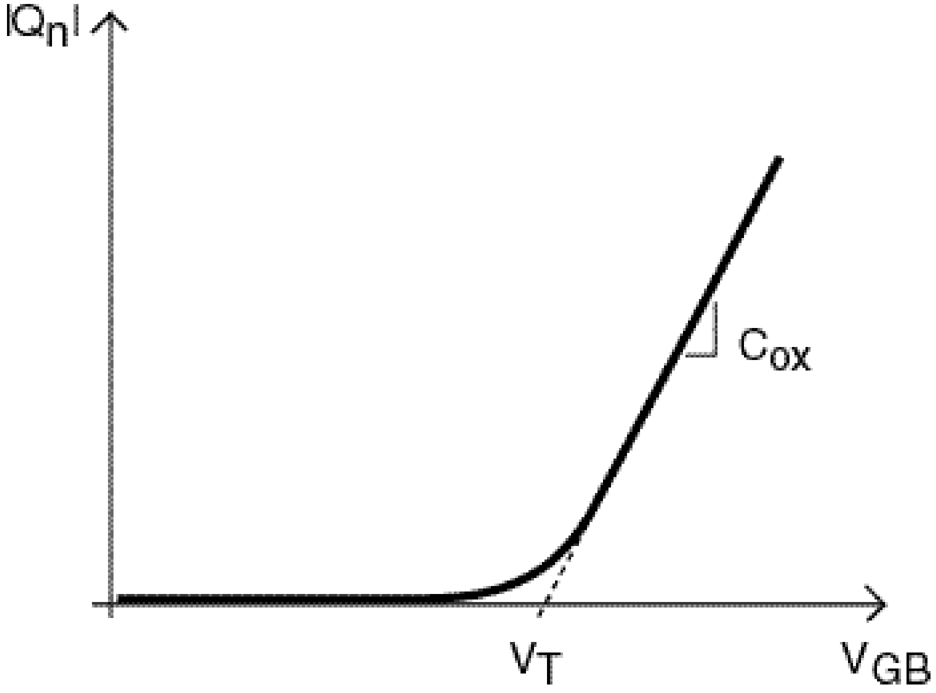
$$Q = CV$$

$$\Rightarrow$$

$$Q_n = -C_{ox}(V_{GB} - V_T) \qquad \text{for } V_{GB} > V_T$$

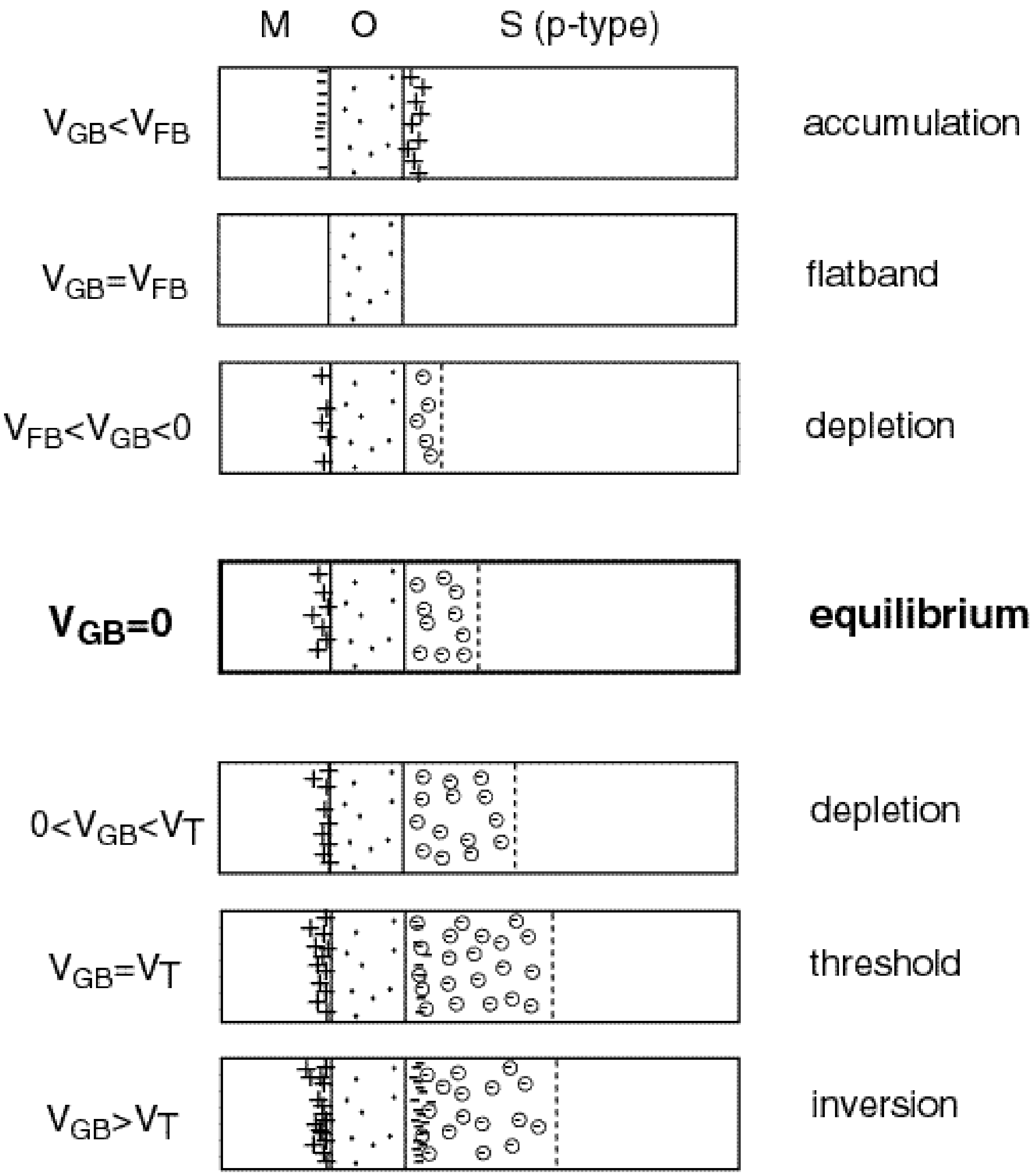
Coul/cm^2

Existence of Q_n and control over Q_n by V_{GB}
$\Rightarrow$ key to MOS electronics



What did we learn today?

Summary of Key Concepts



In inversion:

$$|Q_n| = C_{ox}\left(V_{GB} - V_T\right) \qquad \textit{for } V_{GB} > V_T$$