Lecture 24

Multistage Amplifiers (I)

MULTISTAGE AMPLIFIER

Outline

1. Introduction
2. CMOS multi-stage voltage amplifier
3. BiCMOS multistage voltage amplifier
4. BiCMOS current buffer
5. Coupling amplifier stages

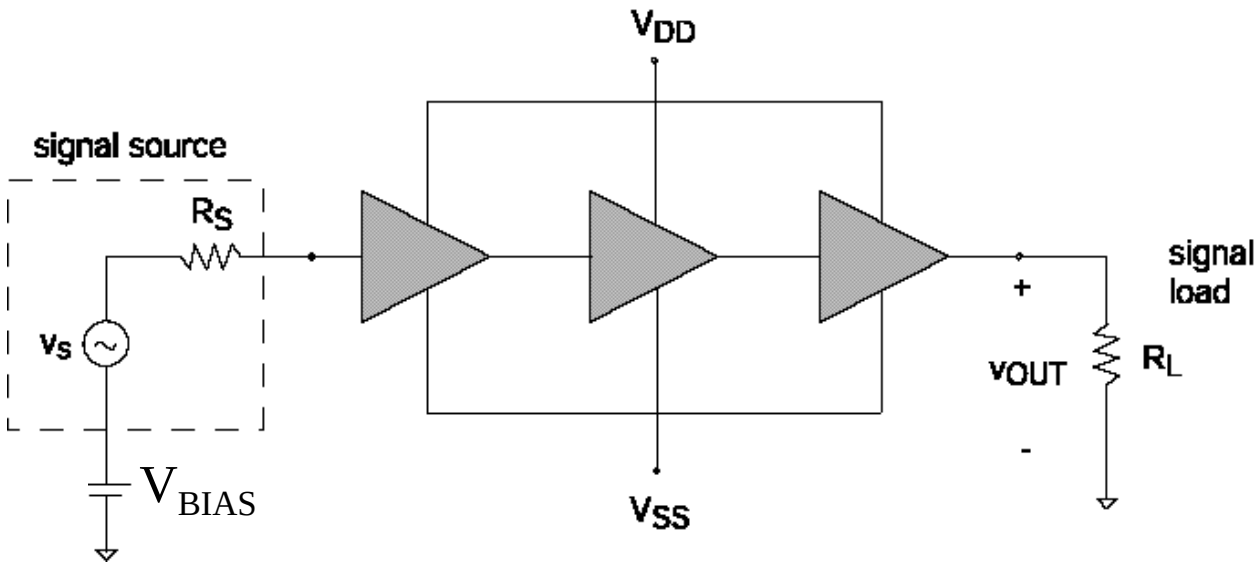
Reading Assignment:
Howe and Sodini, Chapter 9, Sections 9-1-9.3

1. Introduction

Most often, single stage amplifier does not accomplish design goals:

- Need more gain than could be provided by a single stage
- Need to adapt to specified R_S and R_L to maximize efficiency

⇒ ***Multistage amplifier***



Issues:

- What amplifying stages should be used and in what order?
- What devices should be used, BJT or MOSFET?
- How is biasing to be done?

Summary of single stage amplifier characteristics

Stage	A_{vo}, A_{io}	R_{in}	R_{out}	Key Function
Common Source	$A_{vo} = -g_m(r_o // r_{oc})$	∞	$r_o // r_{oc}$	Transcon-ductance amplifier
Common Drain	$A_{vo} \approx \frac{g_m}{g_m + g_{mb}}$	∞	$\frac{1}{g_m + g_{mb}}$	Voltage Buffer
Common Gate	$A_{io} \approx -1$	$\frac{1}{g_m + g_{mb}}$	$r_{oc} // [r_o(1 + g_m R_S)]$	Current buffer
Common Emitter	$A_{vo} = -g_m(r_o // r_{oc})$	r_π	$r_o // r_{oc}$	Transcon-ductance amplifier
Common Collector	$A_{vo} \approx 1$	$r_\pi + \beta_o(r_o // r_{oc} // R_L)$	$\frac{1}{g_m} + \frac{R_S}{\beta_o}$	Voltage buffer
Common Base	$A_{io} \approx -1$	$\frac{1}{g_m}$	$r_{oc} // [r_o(1 + g_m(r_\pi // R_S))]$	Current buffer

Differences between BJT's and MOSFETs

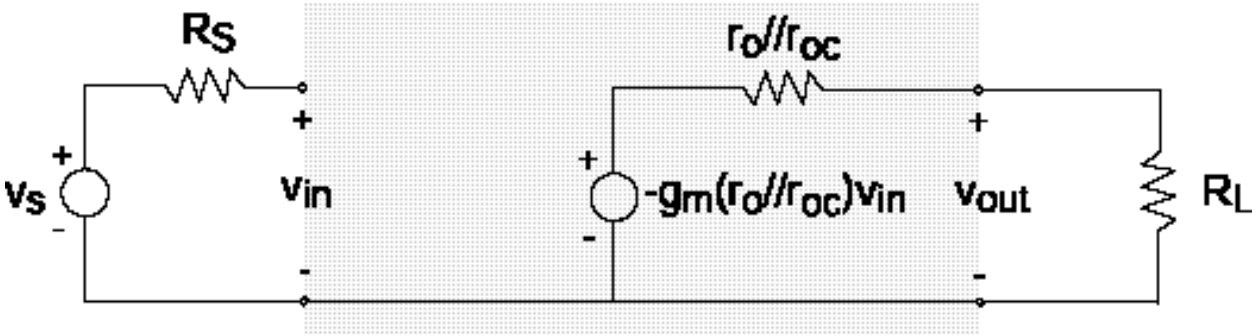
BJT		MOSFET
$r_\pi = \frac{\beta_o}{g_m}$		$g_{mb} \propto g_m$
$g_m = \frac{I_C}{V_{th}}$	>	$g_m = \sqrt{2\frac{W}{L}\mu C_{ox} I_D}$
$r_o = \frac{V_A}{I_C}$	>	$r_o = \frac{1}{\lambda I_D}$

2. CMOS Multistage Voltage Amplifier

Goals:

- High voltage gain, A_{vo}
- High input resistance, R_{in}
- Low output resistance, R_{out}

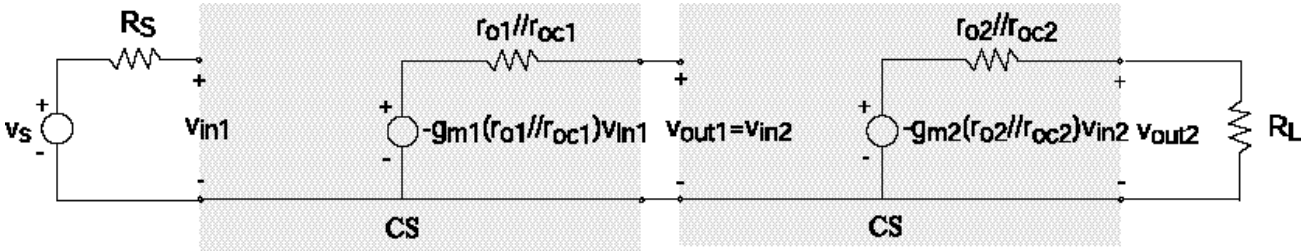
Good starting point: Common-Source stage:



- $R_{in}=\infty$
- $A_{vo}=-g_m(r_o//r_{oc})$, probably insufficient
- $R_{out}= (r_o//r_{oc})$, too high

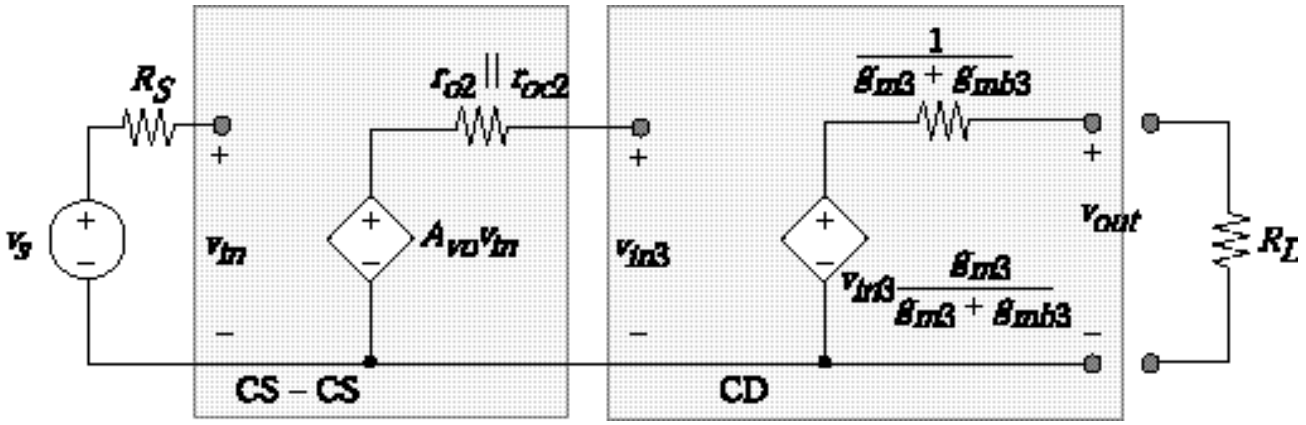
CMOS Multistage Voltage Amplifier (contd.)

Add second CS stage to get more gain:



- $R_{in}=\infty$
- $A_{vo}=g_{m1}(r_{o1}//r_{oc1})\ g_{m2}(r_{o2}//r_{oc2})$
- $R_{out}= (r_{o2}//r_{oc2})$, still too high

Add CD stage at output (to reduce R_{out}):



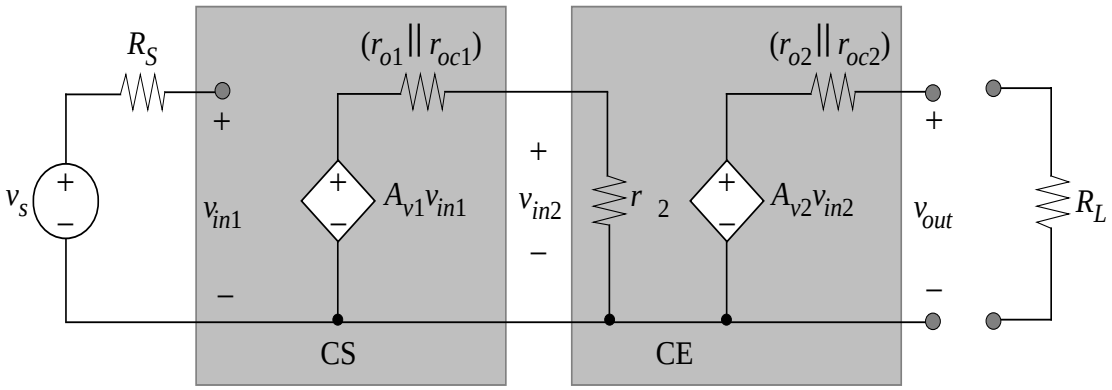
- $R_{in}=\infty$
- $$A_{vo} = g_{m1}(r_{o1} \| r_{oc1})\, g_{m2}(r_{o2} \| r_{oc2})\, \frac{g_{m3}}{g_{m3}+g_{mb3}}$$
- $$R_{out} = \frac{1}{g_{m3}+g_{mb3}}$$

3. BiCMOS multistage voltage amplifier

A_{vo}(CE) > A_{vo}(CS) because r_o(BJT) > r_o(MOSFET), but..

CS stage is best first stage, since $R_{in}=\infty$.

How about adding a CE stage following the CS stage?



However, inter-stage loading degrades gain:

$$R_{out1} = r_{o1} \| r_{oc1} \quad >> \quad R_{in2} = r_{\pi 2}$$

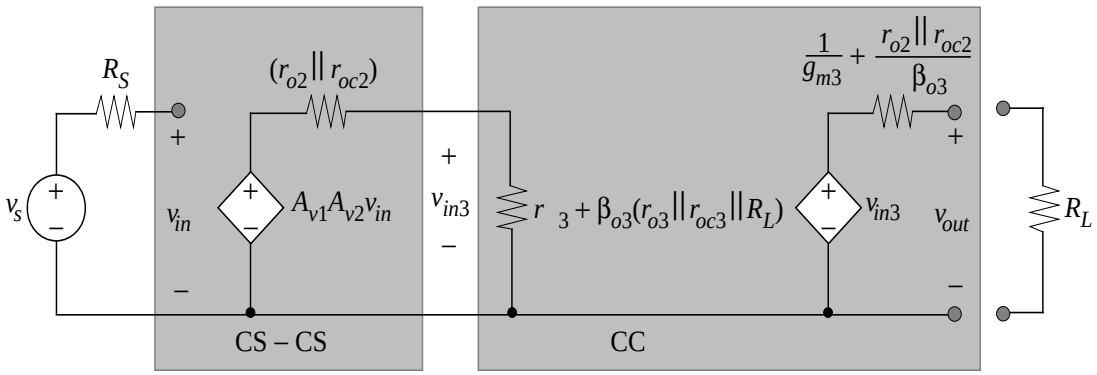
There is a voltage divider between stages

$$\frac{R_{in2}}{R_{out1} + R_{in2}} \approx \frac{R_{in2}}{R_{out1}} \approx \frac{r_{\pi 2}}{r_{o1} \| r_{oc1}} << 1$$

Additional gain provided by the CE stage is mostly lost to inter-stage loading.

BiCMOS multistage voltage amplifier (contd.)

Use two CS stages, but add CC stage at output:



Inter-stage loading:

$$R_{out2} = r_{o2} \| r_{oc2}, \quad R_{in3} = r_{\pi 3} + \beta_{o3}\left(r_{o3} \| r_{oc3} \| R_L\right)$$

Then, inter-stage loss:

$$\frac{R_{in3}}{R_{out2} + R_{in3}} = \frac{r_{\pi 3} + \beta_{o3}\left(r_{o3} \| r_{oc3} \| R_L\right)}{r_{o2} \| r_{oc2} + r_{\pi 3} + \beta_{o3}\left(r_{o3} \| r_{oc3} \| R_L\right)}$$

Better than trying to use a CE stage, but still pretty bad.

The good thing is that R_{out} has improved:

$$R_{out} = R_{out3} = \frac{1}{g_{m3}} + \frac{R_{out2}}{\beta_{o3}} = \frac{1}{g_{m3}} + \frac{r_{o2} \| r_{oc2}}{\beta_{o3}}$$

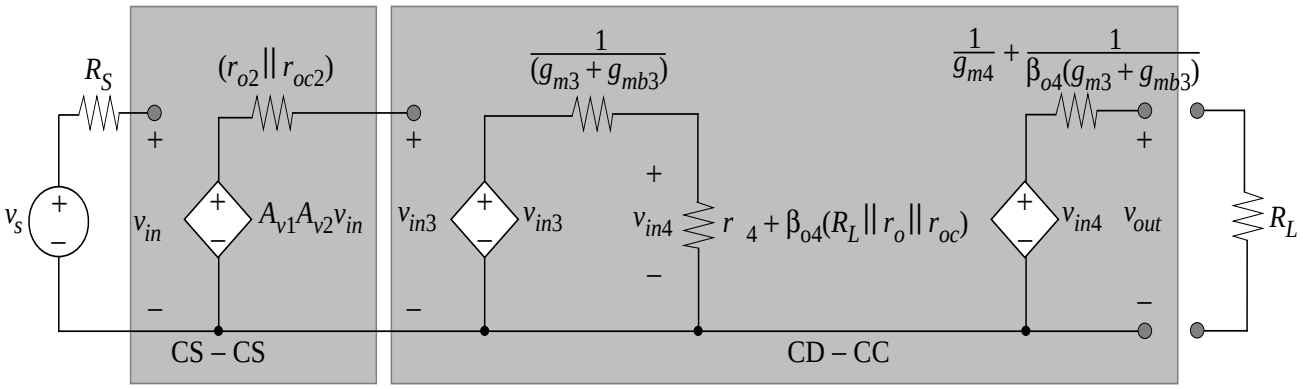
Since, in general g_m(BJT) > g_m(MOSFET), R_{out} could be better than CD output stage if $r_{o2} \| r_{oc2}$ is not too large. Otherwise, CD output stage is better.

BiCMOS multistage voltage amplifier (contd.)

Better voltage buffer: cascade CC and CD output stages

What is the best order?

Since R_{in}(CD)=∞, best to place CD first:



Inter-stage loading:

$$\frac{\boldsymbol{R_{in3}}}{\boldsymbol{R_{in3}} + \boldsymbol{R_{out2}}} = 1$$

$$\frac{\boldsymbol{R_{in4}}}{\boldsymbol{R_{in4}} + \boldsymbol{R_{out3}}} = \frac{\boldsymbol{r_{\pi 4}} + \boldsymbol{\beta_{o4}}\left(\boldsymbol{r_{o4}} \| \boldsymbol{r_{oc4}} \| \boldsymbol{R_L}\right)}{\dfrac{1}{\boldsymbol{g_{m3}} + \boldsymbol{g_{mb3}}} + \boldsymbol{r_{\pi 4}} + \boldsymbol{\beta_{o4}}\left(\boldsymbol{r_{o4}} \| \boldsymbol{r_{oc4}} \| \boldsymbol{R_L}\right)} \approx 1$$

The output resistance is excellent:

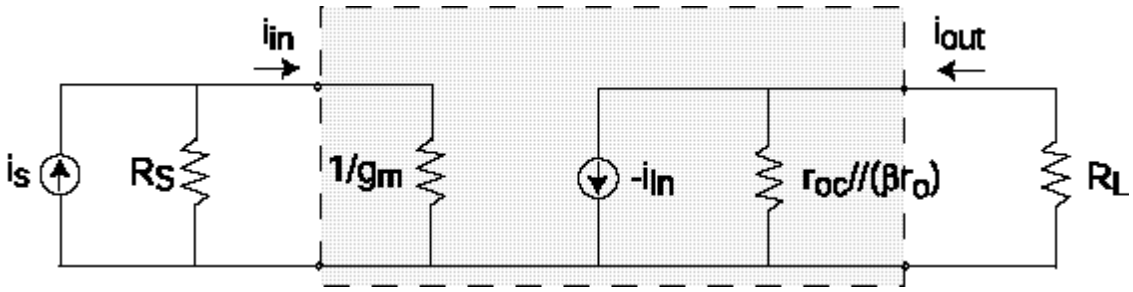
$$\boldsymbol{R_{out}} = \boldsymbol{R_{out4}} = \frac{1}{\boldsymbol{g_{m4}}} + \frac{\boldsymbol{R_{out3}}}{\boldsymbol{\beta_{o4}}} = \frac{1}{\boldsymbol{g_{m4}}} + \frac{1}{\boldsymbol{\beta_{o4}}\left(\boldsymbol{g_{m3}} + \boldsymbol{g_{mb3}}\right)}$$

4. BiCMOS current buffer

Goals:

- Unity current gain, A_i=1
- Very low input resistance, R_{in}
- Very high output resistance, R_{out}

Start with a common-base stage:



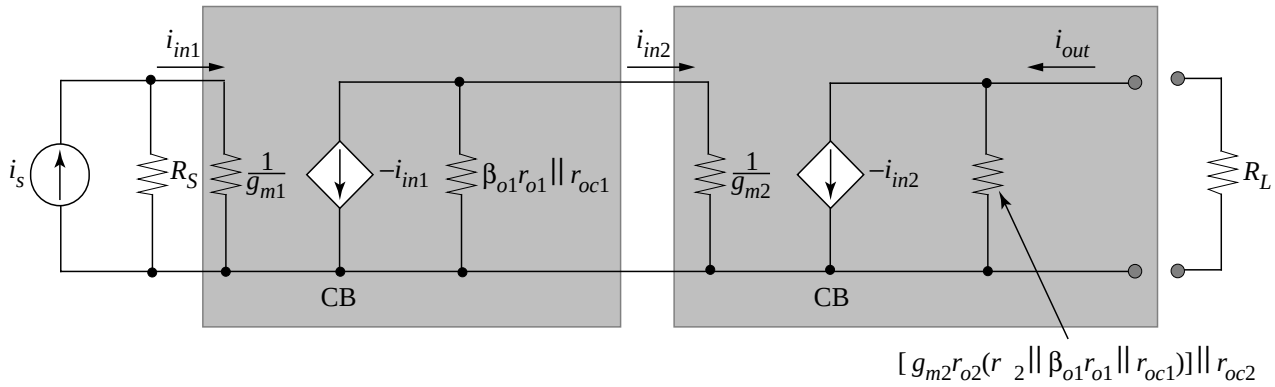
- $A_{io} = -1$
- $R_{in} = \dfrac{1}{g_m}$
- $R_{out} = r_{oc} \parallel \left\{ r_o \left[1 + g_m \left(r_\pi \parallel R_S \right) \right] \right\}$

Note that if R_S is "high enough", $R_{out} \approx r_{oc} \| (\beta_o r_o)$.

Can we increase R_{out} further by adding a second CB stage?

BiCMOS current buffer (contd).

CB-CB Current Buffer



Now

$$R_{out} = R_{out2} = r_{oc2} \| \left\{ r_{o2} \left[1 + g_{m2} \left(r_{\pi 2} \| R_{out1} \right) \right] \right\}$$

Plugging in $R_{out1} \approx r_{oc1} \| (\beta_{o1} r_{oc1})$.

$$R_{out} = r_{oc2} \| \left\{ r_{o2} \left[1 + g_{m2} \left(r_{\pi 2} \| r_{oc1} \| \beta_{o1} r_{o1} \right) \right] \right\}$$

But, since $r_{\pi 2} << r_{oc1} \| (\beta_1 r_{oc1})$, then

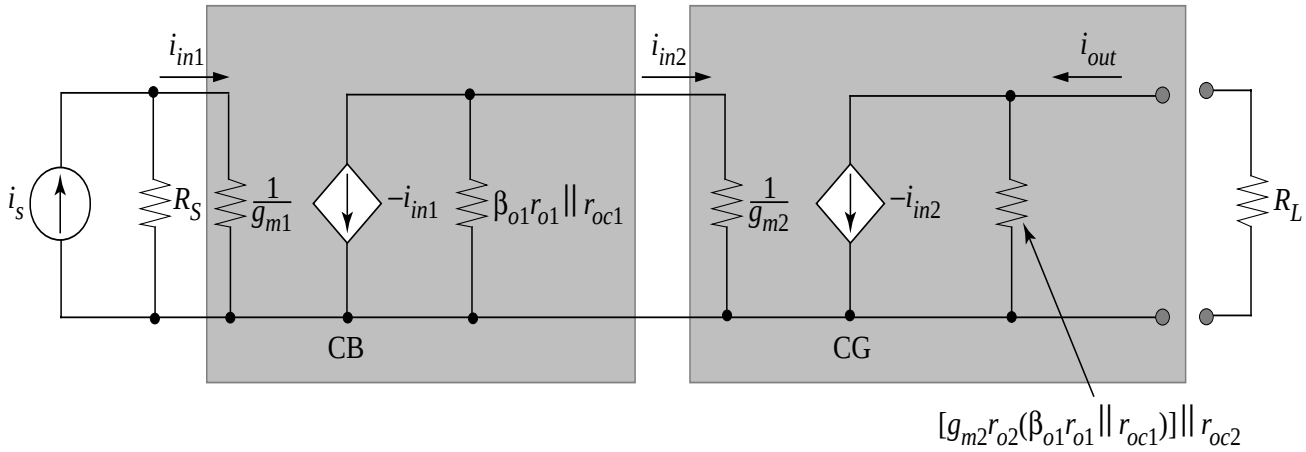
$$R_{out} = r_{oc2} \| \left[r_{o2} \left(1 + g_{m2} r_{\pi 2} \right) \right] \approx r_{oc2} \| \left(\beta_{o2} r_{o2} \right)$$

Did not improve anything! The base current limits the number of CB stages that can improve the output resistance to just one.

Since the CG stage has no gate current, cascade it with the CB stage

BiCMOS current buffer (contd).

CB-CG Current Buffer



$$R_{out} = R_{out2} = r_{oc2} \| \left[r_{o2}\left(1 + g_{m2}R_{out1}\right) \right]$$

Plugging in $R_{out1} \approx r_{oc1} \| (\beta_{o1} r_{oc1})$.

$$R_{out} = r_{oc2} \| \left[r_{o2} g_{m2} \left(r_{oc1} \| \beta_{o1} r_{o1} \right) \right]$$

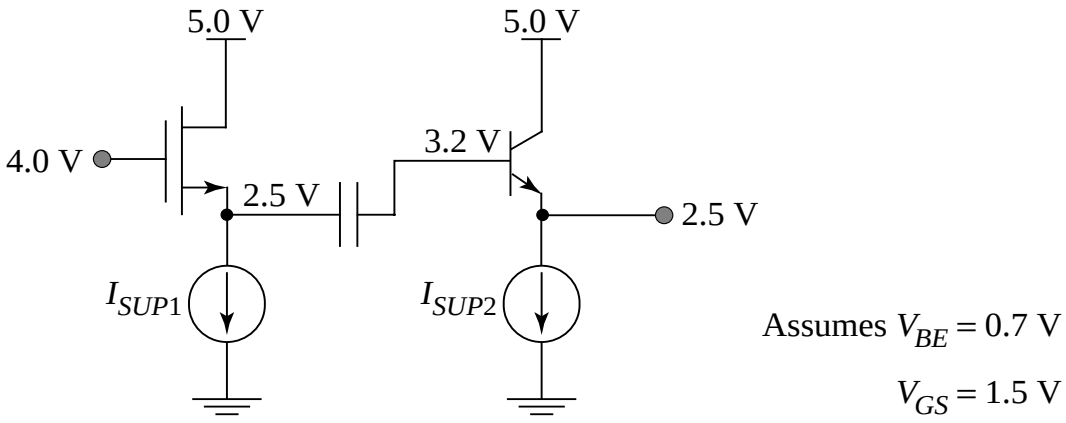
Now R_{out} has improved by about $g_{m2}r_{o2}$, but only to the extent that r_{oc2} is high enough…

5. Coupling Amplifier Stages

CAPACITIVE COUPLING

Capacitors that have large enough value behave as AC short, so the signal goes through but bias is independent for each stage.

Example, CD-CC voltage buffer:

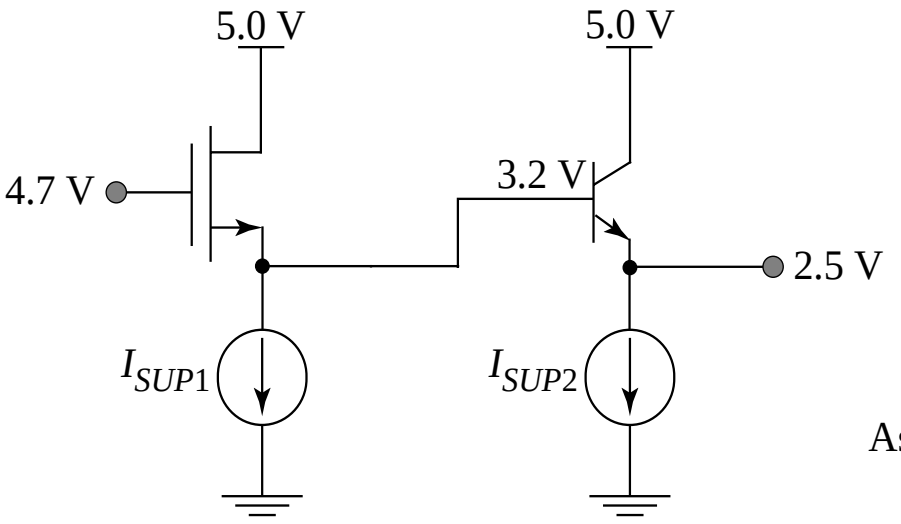


- Advantages
  - Can select bias point for optimum operation
  - Can select bias point close to the mid-point of the power rails for maximum voltage swing
- Disadvantages
  - To approximate AC short, large capacitors are needed and they consume large area.

Coupling Amplifier Stages (contd.)

DIRECT COUPLING: share bias points across stages.

Example, CD-CC voltage buffer:



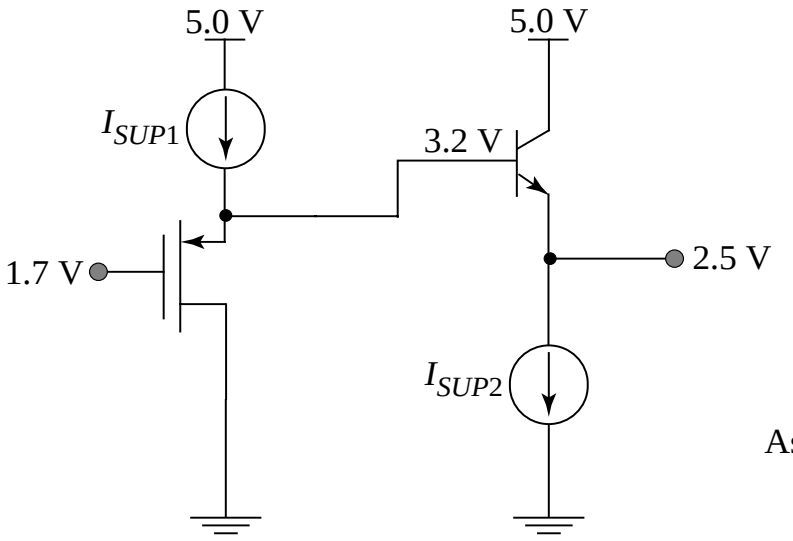
Assumes $V_{BE} = 0.7$ V

$V_{GS} = 1.5$ V

- Advantages
  - No capacitors needed
  - compact
- Disadvantages
  - Bias point shared:constrains designs.
  - Bias shifts from stage to stage and can stray too far from center of range
  - Generally requires level shifting to bring signal back to center of range.

Coupling Amplifier Stages (contd.)

SOLUTION: use PMOS CD stage for level shifting.

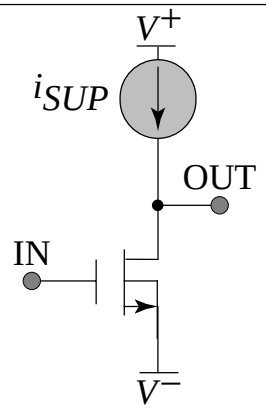
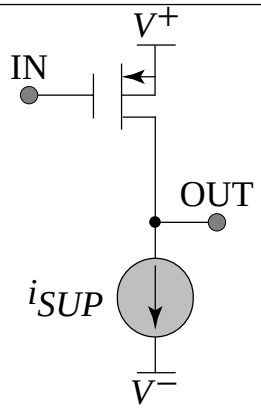
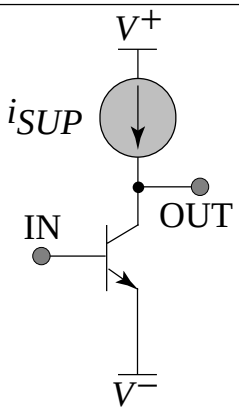
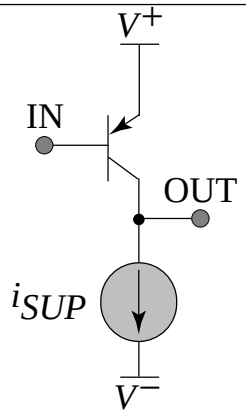
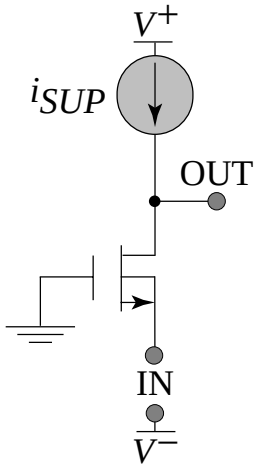
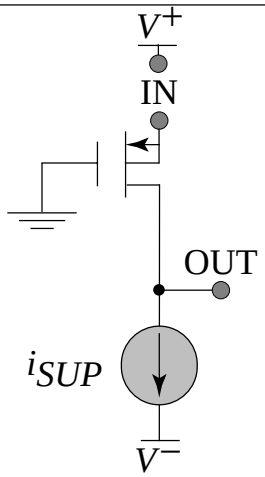
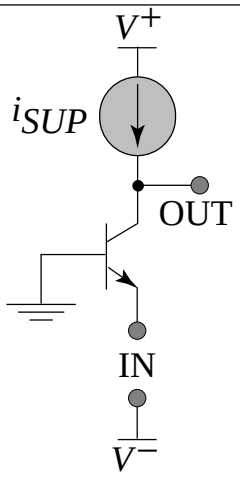
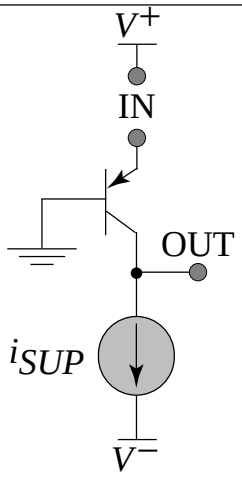
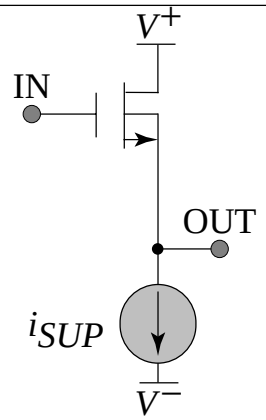
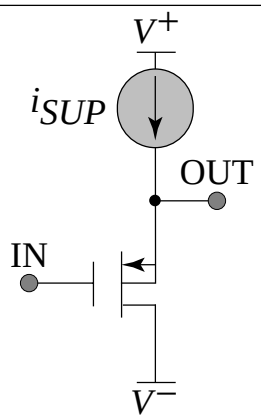
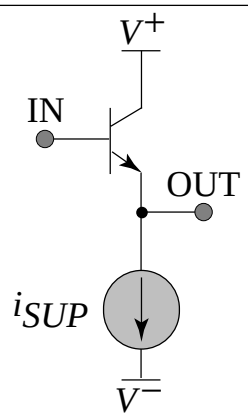
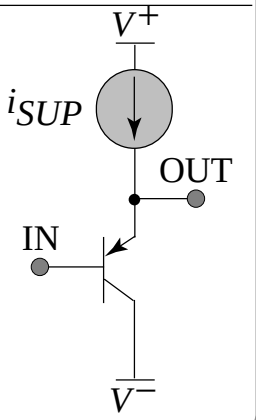


Assumes $V_{BE} = 0.7$ V

$V_{GS} = 1.5$ V

Coupling Amplifier Stages (contd.)

Summary of DC shifts through amplifier stages:

Amplifier Type	Transistor Type			
	NMOS	PMOS	npn	pnp
Common Source/ Common Emitter (*CS*/*CE*)				
Common Gate/ Common Base (*CG*/*CB*)				
Common Drain/ Common Collector (*CD*/*CC*)				

What did we learn today?

Summary of Key Concepts

- To achieve design goals, multistage amplifiers are often needed
- In multistage amplifiers, different stages are used to accomplish different goals
  - **Voltage gain**: common-source, common emitter
  - **Voltage buffer**: common drain, common collector
  - **Current buffer**: common gate, common base
- In multistage amplifiers, attention must be paid to inter-stage loading to avoid unnecessary losses
  - Must select compromise bias,
  - Must pay attention to bias shift from stage to stage