Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science
6.012
Microelectronic Devices and Circuits
Spring 2007
February 21, 2007 - Homework #2
Due - February 28, 2007

Problem 1

Fill in the values for the maximum absolute electric field, built in voltage, and depletion width for the following pn junctions. Assume thermal equilibrium.

N_d cm^{-3}	N_a cm^{-3}	x_{no} nm	x_{po} nm	E_o kV/cm	ϕ_{bi} mV
10^{15}	10^{15}	**623**	**623**	**9.6**	**600**
10^{16}	10^{17}	**303**	**30.3**	**46.8**	**780**
10^{16}	10^{18}	**328**	**3.28**	**50.7**	**840**

$\phi_{bi} = 60\text{ mV} \log(N_d N_a/n_i^2)$
$x_p = [(2\,\varepsilon_s\,\phi_{bi}\,N_d)(q\,N_a\,(N_a + N_d))^{-1}]^{0.5}$
$x_n = x_p\,N_a/\,N_d$
$E = q\,x_n\,N_d\,/\varepsilon_s$

Compare these values to Example 3.4 in the text and figure out what resulted in the differences.

Problem 2

We have a PN junction with the p-type side doped with $N_a = 10^{17}$ cm^{-3} and the n-type side doped with $N_d = 10^{18}$ cm^{-3}. Assume thermal equilibrium.

a) Compute the built in potential ϕ_{bi}.
b) Calculate the depletion width on each side: x_{n0} and x_{p0}.
c) Plot the charge density, electric field, and electric potential across the PN junction. Please follow the graph convention in Howe & Sodini.

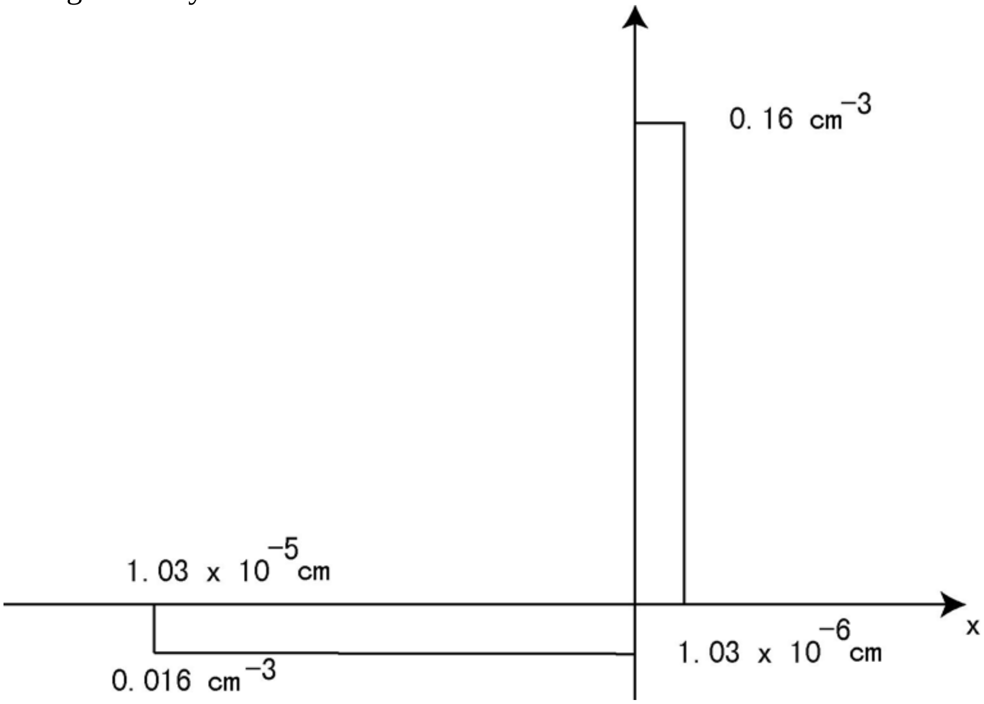
a) $\phi_{bi} = v_{th} \ln(N_a N_d/n_i^2)$ = **0.898 V**
b) Using Eq 3.55
$x_{n0} = [(2 \times 1.035\text{x}10^{-12} \times .898 \times 10^{17})(1.6\text{x}10^{-19} \times 10^{18} \times (10^{17} + 10^{18}))^{-1}]^{0.5}$ = **1.03x10-6 cm**
Using Eq 3.52
x_{p0} = **1.03x10^{-5} cm**

c) $E_{max} = -\,qN_a x_{p0}/\varepsilon_s = -159$ kV/cm
$\phi_n = v_{th} \ln(N_d/n_i) = .479$
$\phi_p = v_{th} \ln(N_a/n_i) = -.419$

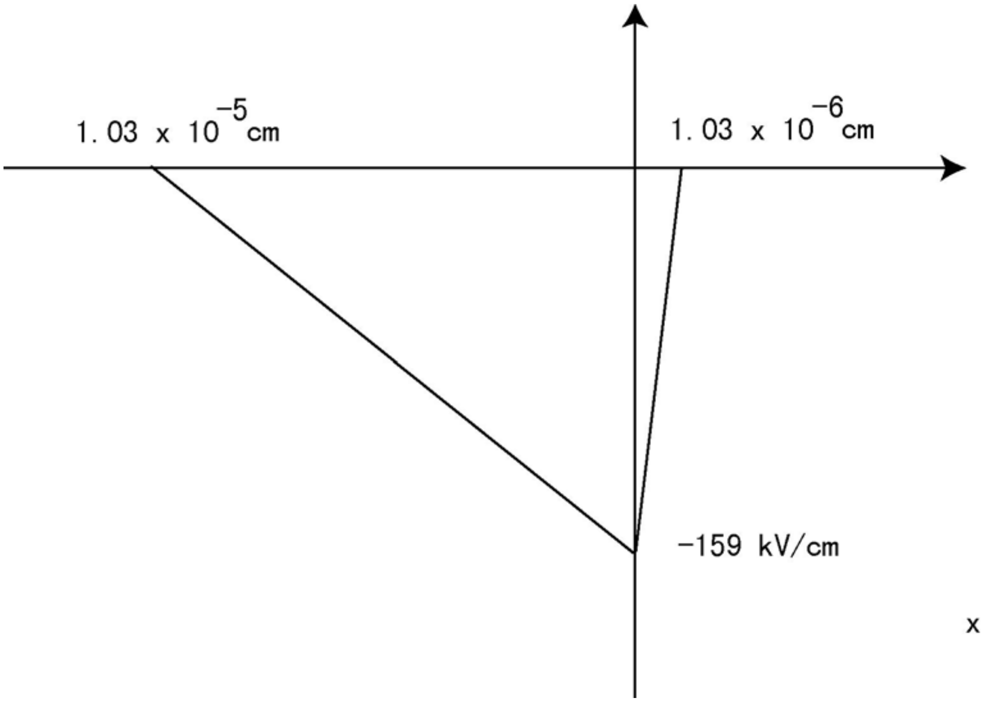
$\phi(0) = \phi_n - E_{max}\, x_{n0}/2 = .397$

In addition to x_{p0} and x_{n0}, these are the only six numbers needed for the graphs.

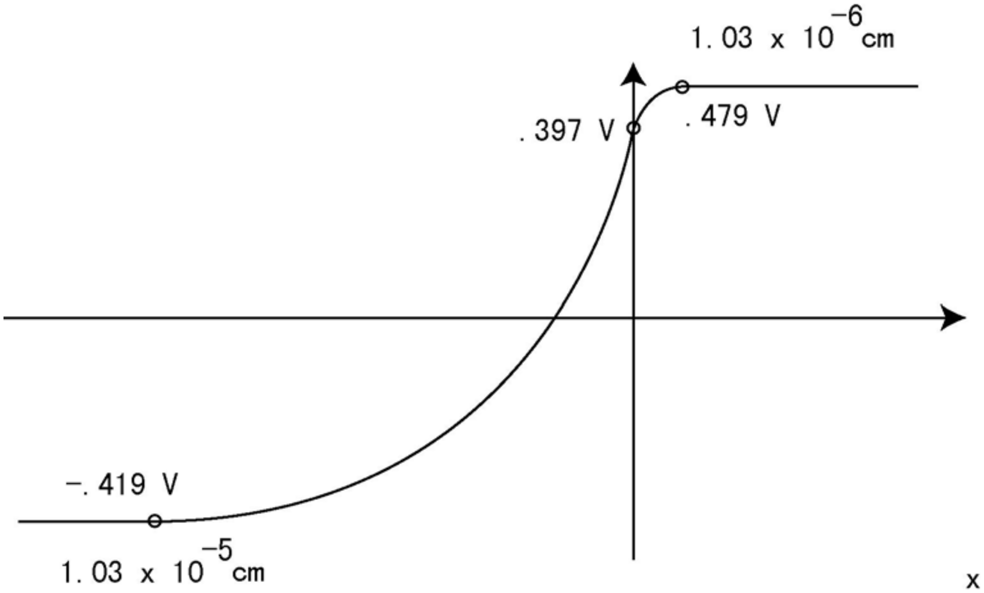
Charge Density



Electric Field

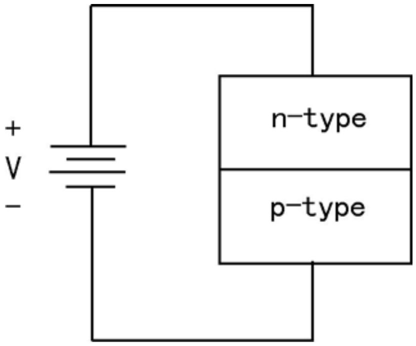


Potential



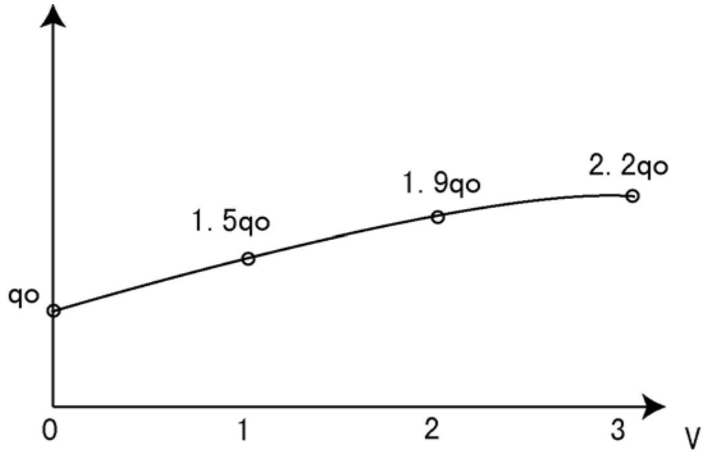
Problem 3

Given x_{no} = 100 nm, ϕ_{bi} = 780 mV, $N_d = 10^{17}$ cm^{-3}. The voltage V varies from 0 to +3 volts.



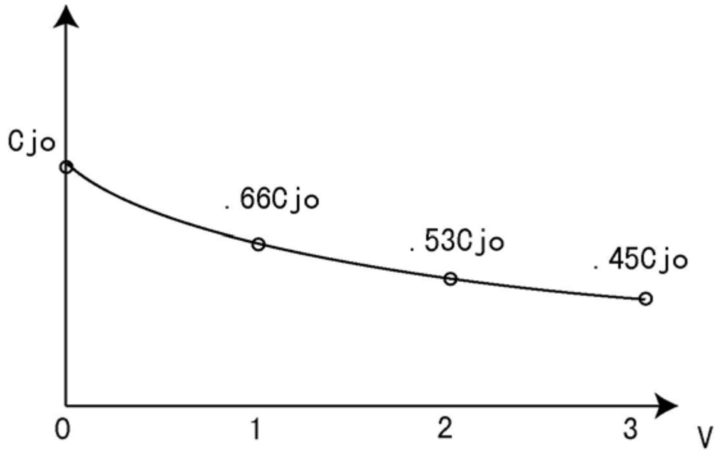
a) Plot the amount of charge stored on the n-side versus voltage V.
b) What is C_{jo}, the depletion capacitance at zero bias? Plot C_j versus voltage V.

a) $q_o = q\, x_{no}\, N_d = 1.6\text{x}10^{-7}$ coulombs/cm^2
$q(V) = q_o\,(1+(V/\phi_{bi}))^{0.5}$



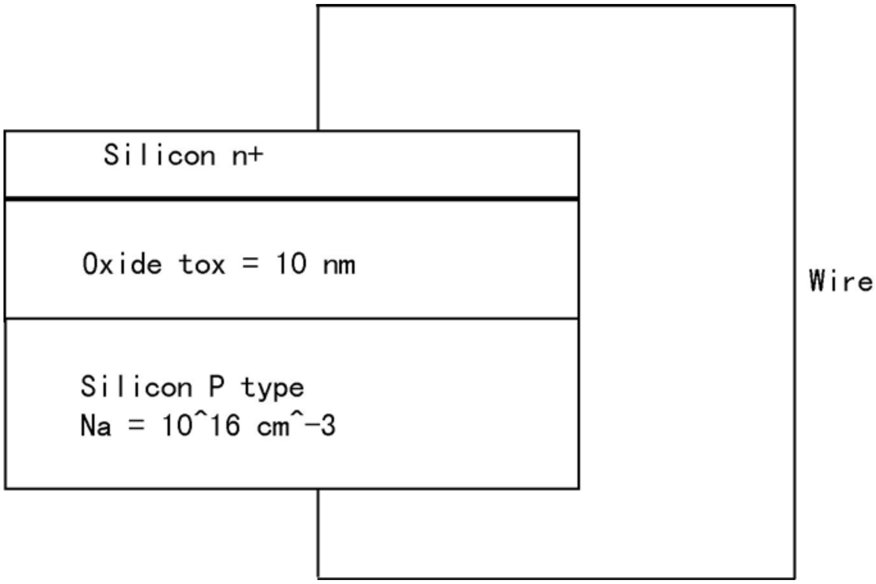
b) $C_{jo} = q\, x_{no}\, N_d / 2\phi_{bi} = 10^{-7}$ farads/cm^2

$C_j(V) = C_{jo}(1+(V/\phi_{bi}))^{-.5}$



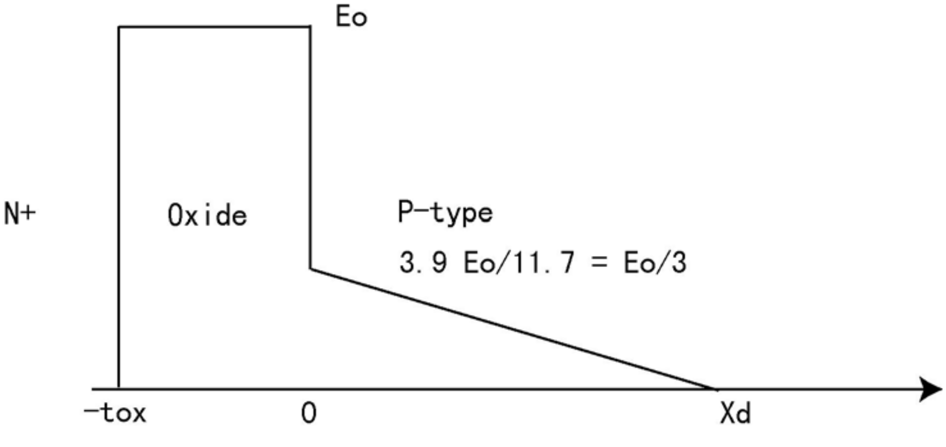
Problem 4

For the given set up:



a) Plot the electric field versus distance. Follow the convention in H&S. Set the oxide and p-type interface as x = 0.
b) Plot the charge density versus distance.

a) ϕ_{n+} = 550 mV and ϕ_p = -60 mV log($10^{16}/10^{10}$) = -360 mV
There is a total voltage drop of 910 mV across the MOS. We know there will be charge at the boundary of the oxide and the n+ silicon, no charge in the oxide, and a constant charge density of qN_a in the depleted region of the p-type silicon. Since the electric field is proportional to the integral of charge it will look like this.



The field decreases at a linear rate in the silicon because the charge density is constant. Using E = q$N_a$$X_d$/$\varepsilon_s$, we know X_d = ε_s Eo/3qN_a. Since the voltage is the negative integral of the electric field we know that:
.91 = Eo x tox + ½ x X_d x Eo/3 (area of a triangle) = Eo x tox + $Eo^2\varepsilon_s$ /18qN_a
Using the quadratic formula, Eo = 157.7 kV/cm and X_d = 340 nm.

b) To maintain charge neutrality, the charge on the metal surface is the opposite of the total charge in the silicon. The total charge in the silicon is $-qN_aX_d = -5.44 \times 10^{-8}$ coulombs cm^{-2}.